

Introduction to HKUST/CAMP/EPACK Lab

*Electronic Packaging Laboratory
Center for Advanced Microsystems Packaging
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先進微系統封裝中心
Center for Advanced Microsystems Packaging



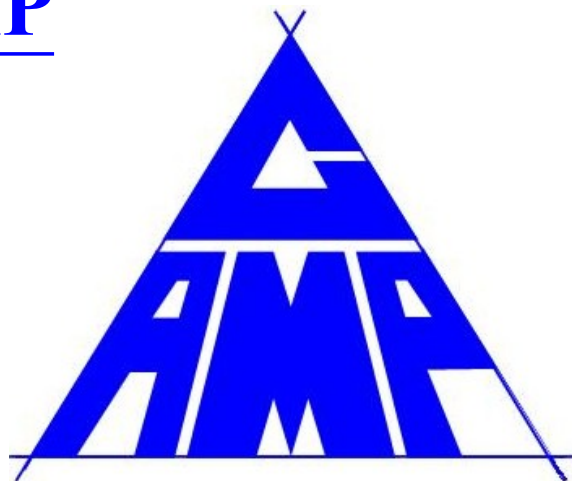
Hong Kong University of Science and Technology



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Center for Advanced Microsystems Packaging

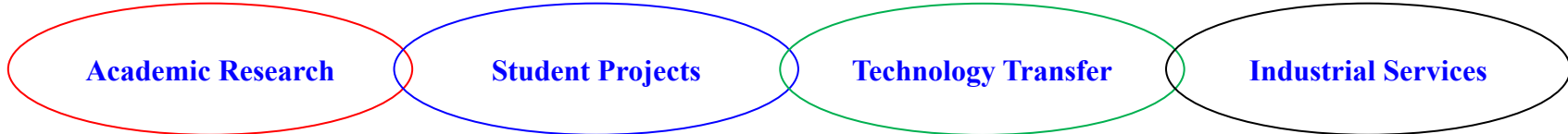


EPACK Lab / CAMP



**Center for Advanced Microsystems Packaging
(CAMP)**

**Electronic Packaging Laboratory
(EPACK Lab)**



Prof. S. W. Ricky LEE
Director

Dr. Jeffery C. C. LO
Assistant Director

Justina KO
Clerk

Dr. Mian TAO
Senior Technical Officer

Professor: 1
PhD: 3
Post-graduate students: 4



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R&D and Technical Services

Wafer Level Processes

- Mask Design and Fabrication
- Thin Film Deposition
- Photolithography
- Dry/Wet Etching
- Plating (TSV, UBM, Solder, etc)
- Wafer dicing

Chip/Package Level Processes

- Die Bonding (Adhesive, Eutectic)
- Wire Bonding (Au, Al, Cu)
- Flip Chip Bonding (Thermo-compression, Thermo-sonic)
- Underfill, Molding & Encapsulation

Board Level Processes

- Substrate and PCB Layout
- SMT
- Rework

Simulation

- Mechanical
- Thermal
- Thermo-mechanical
- Optical

Reliability Assessment

- Thermal Cycling
- HAST
- Moisture Sensitivity Level
- Microtesting (Die Shear, Ball Pull/Shear, Wire Pull/Shear)
- Bending (Monotonic, Cycling)
- Drop Test

Failure Analysis

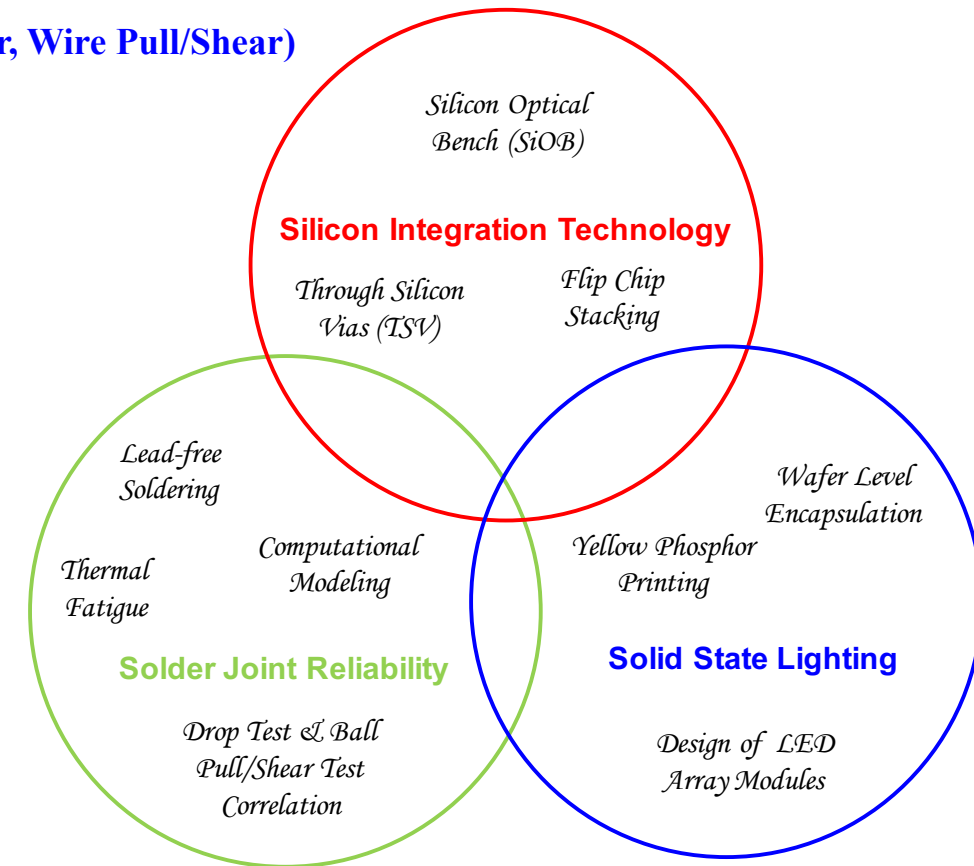
- X-Ray & C-SAM
- Cross-section Inspection
- SEM/EDX Inspection

Material Characterizations and Inspection

- DSC, DMA, TMA, TGA
- Thermal Conductivity Measurement
- All UTM Related Testing
- Roughness, Warpage Measurement

Optical/Thermal Characterization

- Integrating Sphere
- Goniophotometer
- Fluorescence Spectrometer
- Thermal Transient Tester



Research Projects

- **Additive Manufacturing for Advanced Microsystems Packaging**

- Polymer core copper pillar
- Redistribution Layers

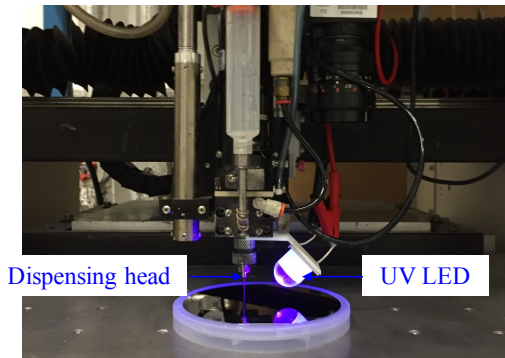
- **LED Packaging**

- LED System-in-Package
- White Light LED SPD Prediction
- Thermal Management for High Power LEDs
- UV LED Packaging

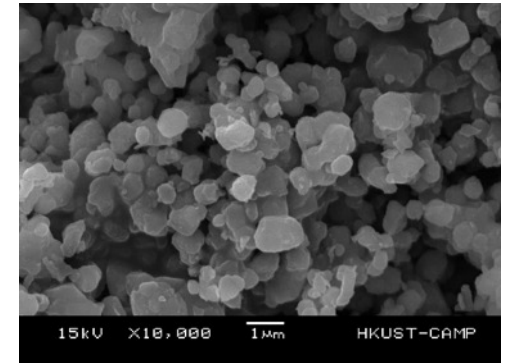
- **Solder Joint Reliability**

- Correlation of Joint and Board Level Reliability

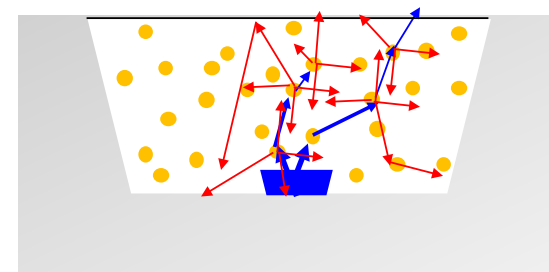
- **Implantable Medical Device Packaging**



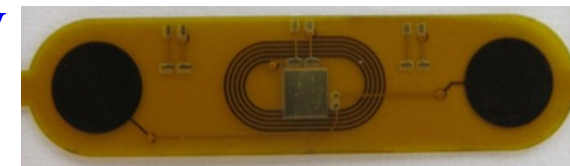
Instant Epoxy Curing System



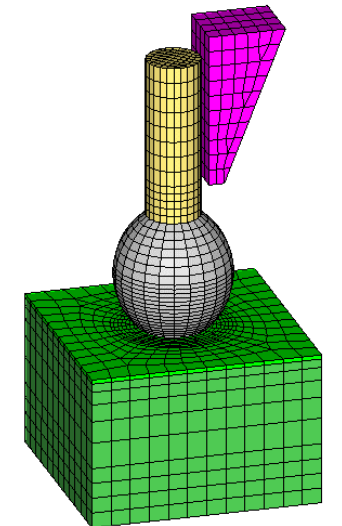
High Thermal Conductivity Underfill



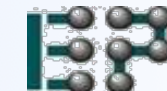
LED SPD Prediction



Implantable Medical Device



Pin Shear Test Simulation

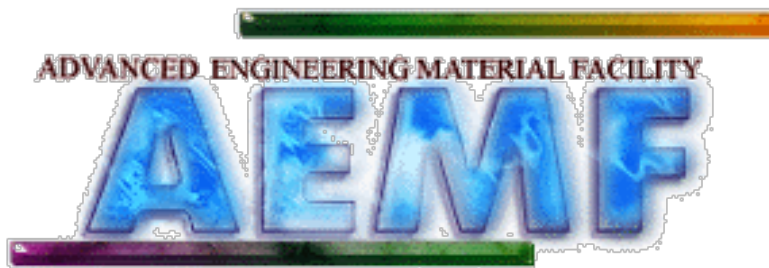


Partners @ HKUST



Materials Characterization & Preparation Facility (MCPF)

www.mcpf.ust.hk



www.aemf.ust.hk



Nano Fabrication Facilities (NFF)

www.nff.ust.hk



www.dmsf.ust.hk



HKUST LED-FPD Tech. R&D Center at Foshan

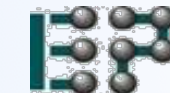
www.fslldctr.org

Semiconductor Product Analysis and Design Enhancement (SPADE) Center

www.spade.ust.hk



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Funding Sources and Industrial Partners

- **Research Grant Council (RGC)**
- **Innovation and Technology Fund (ITF)**
 - Midstream and downstream R&D projects
 - Collaborate with industrial partners
- **Industrial Services**
- **Collaborative R&D Projects**
- **Engineering-Industrial Consortium (EIC) Membership**

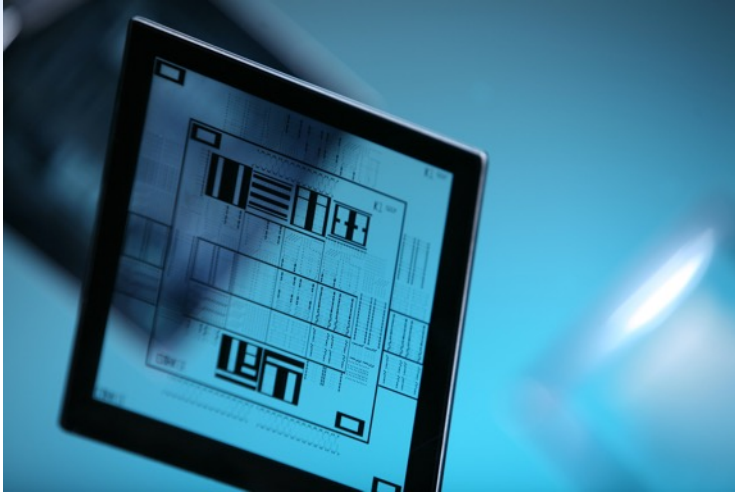


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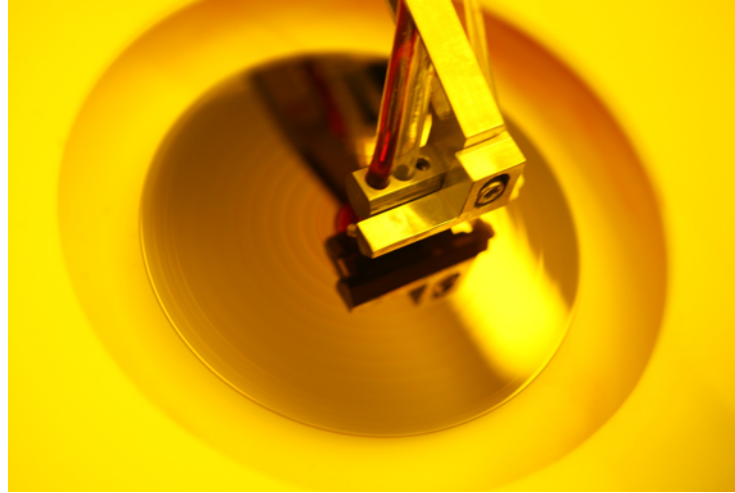


Photolithography

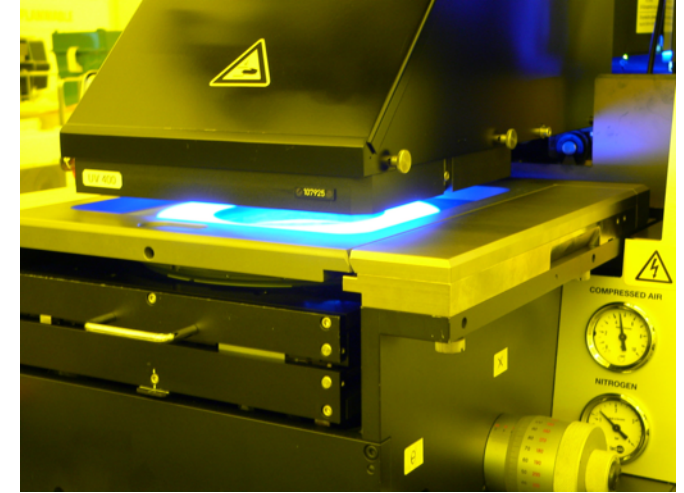
Source: NFF @ HKUST



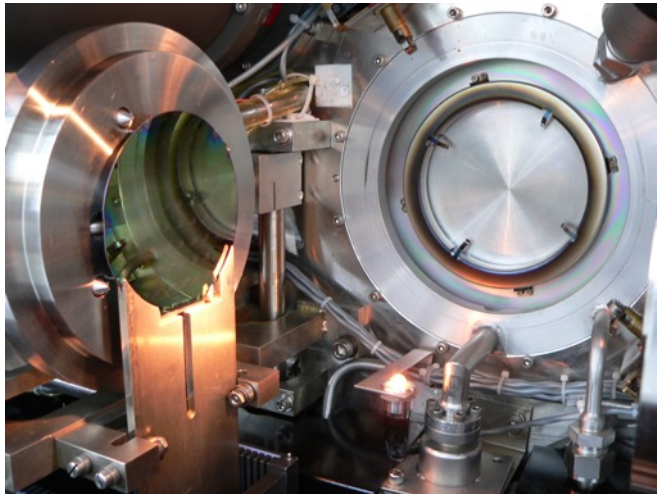
Mask Making



Photoresist Coating (Spin/Spray Coating)



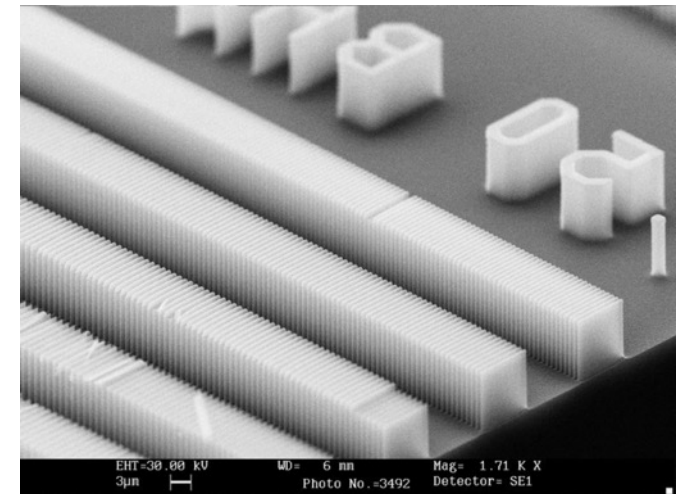
Contact Aligner



Thin Film Deposition



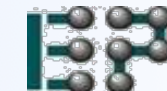
Wet Process



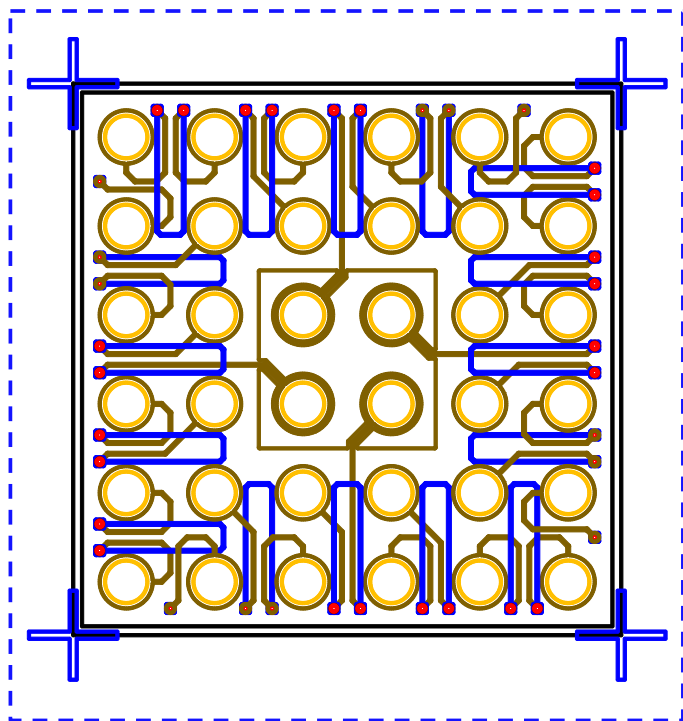
Dry Etching



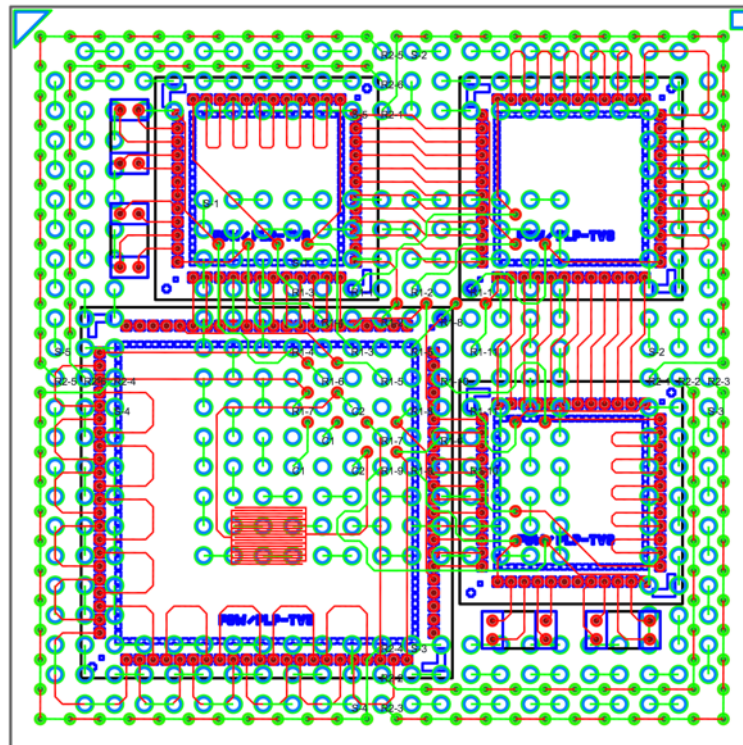
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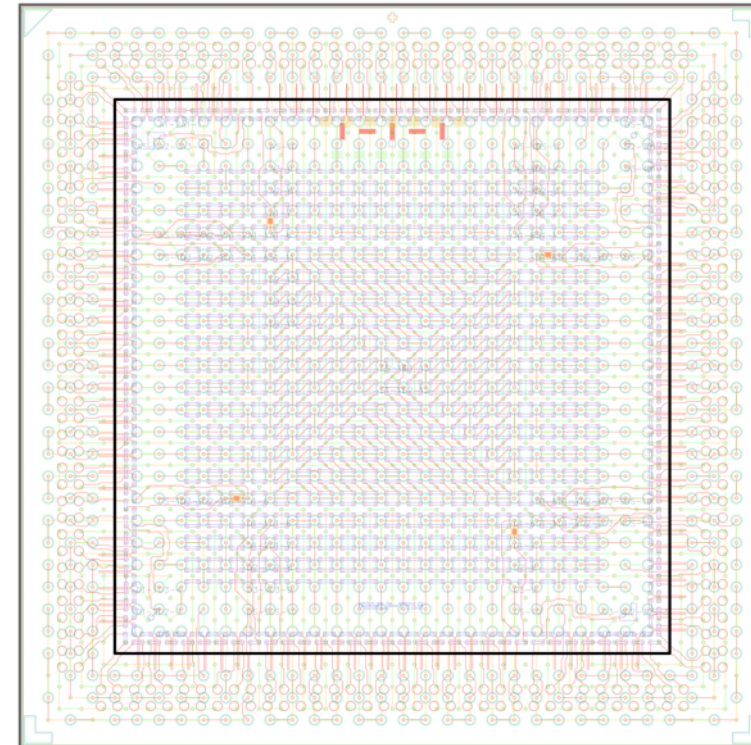
Wafer Level Process (Mask Design)



Fan-in WLCSP
1 RDL Layer



Fan-out WLP (SiP)
2 RDL Layers



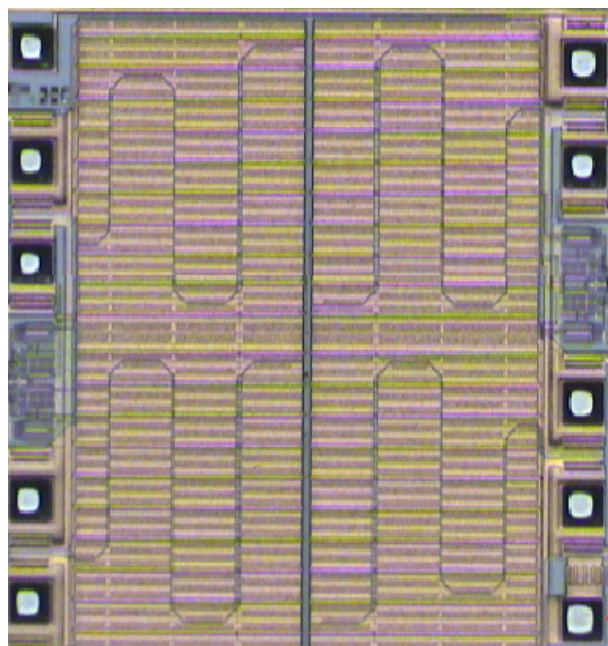
Fan-out WLP
3 RDL Layers



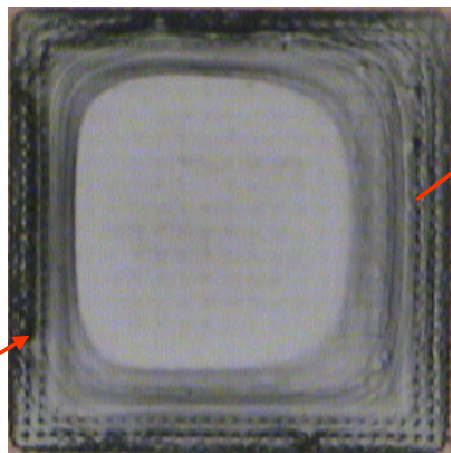
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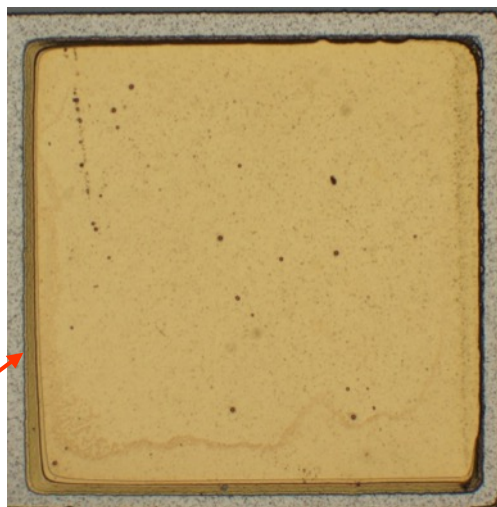
Electro-/Electroless Plating



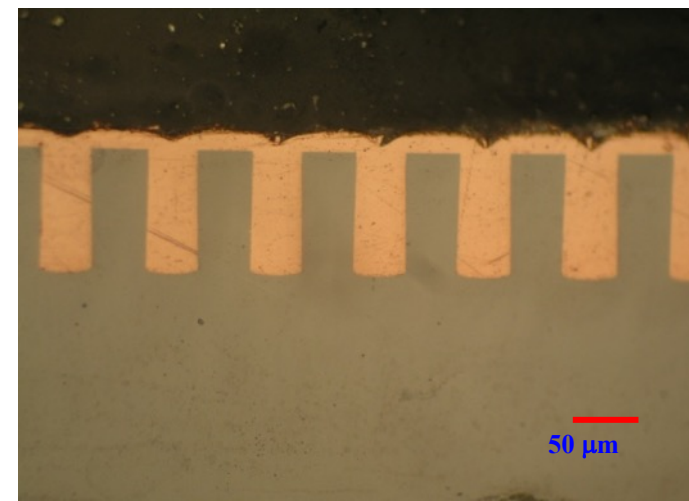
IC with Al Pad



Electroless Nickel Plating



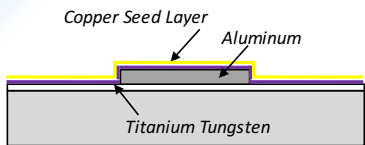
Electroless Gold Plating



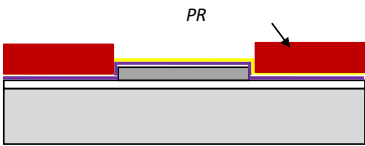
TSV Plating



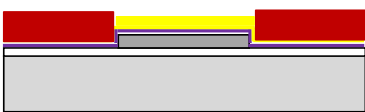
Wafer Level Bumping



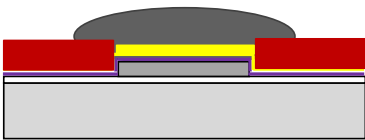
Deposition of Adhesion and Seed Layer



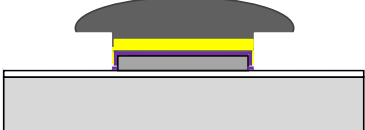
Thick PR Mask Patterning



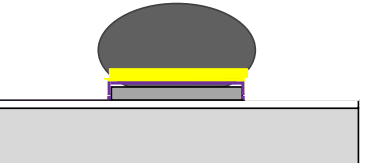
Electro-Copper Plating



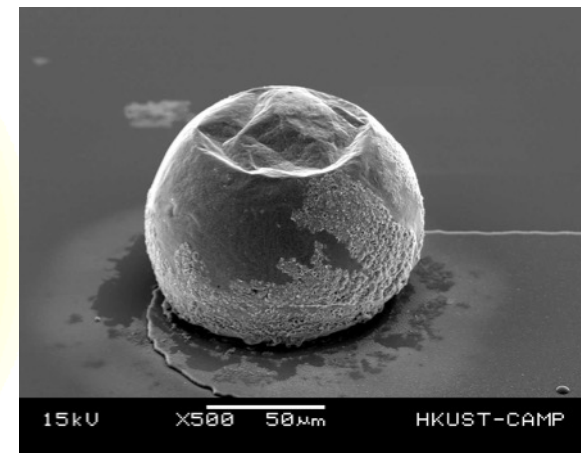
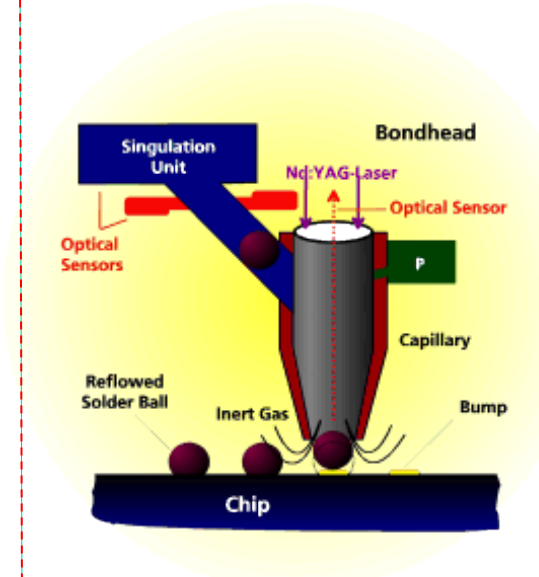
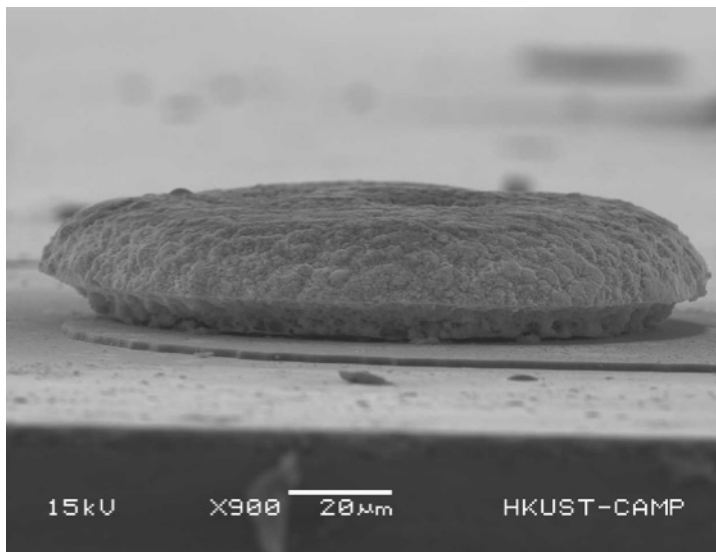
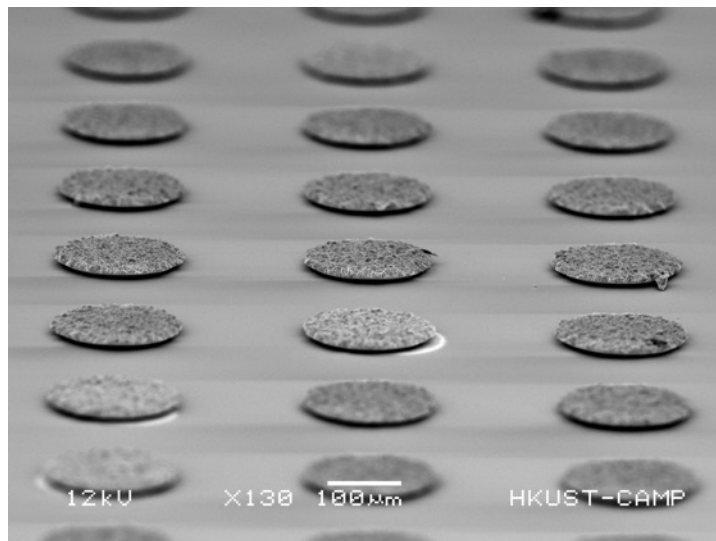
Solder Plating



PR Stripping and Seed Layer Etching



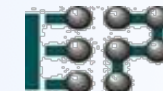
Reflow



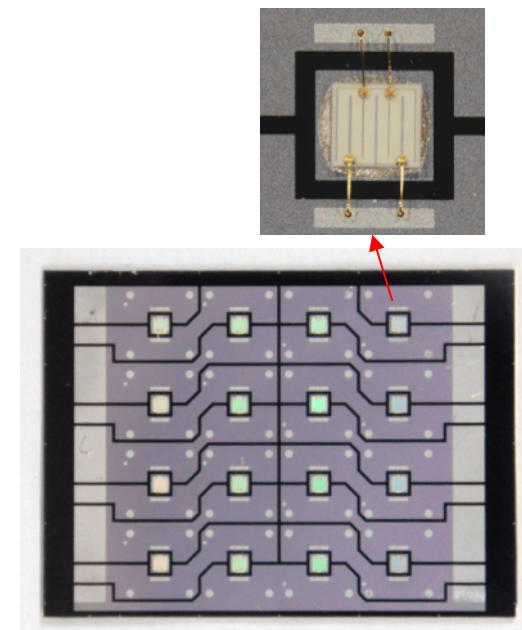
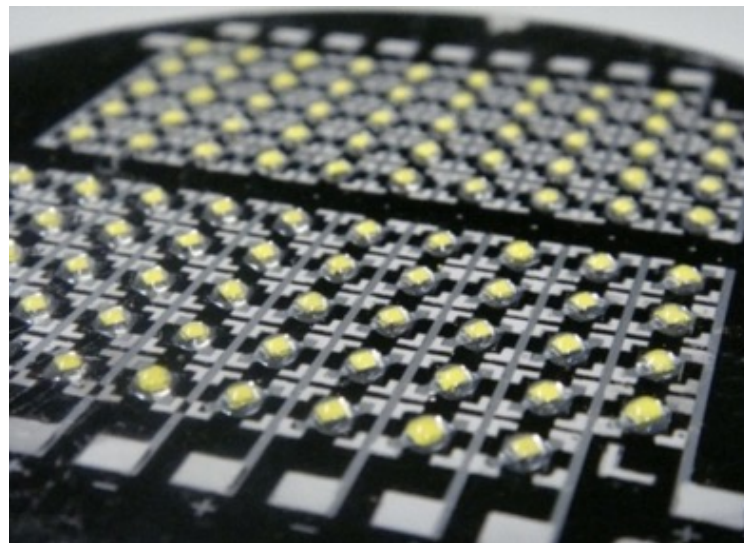
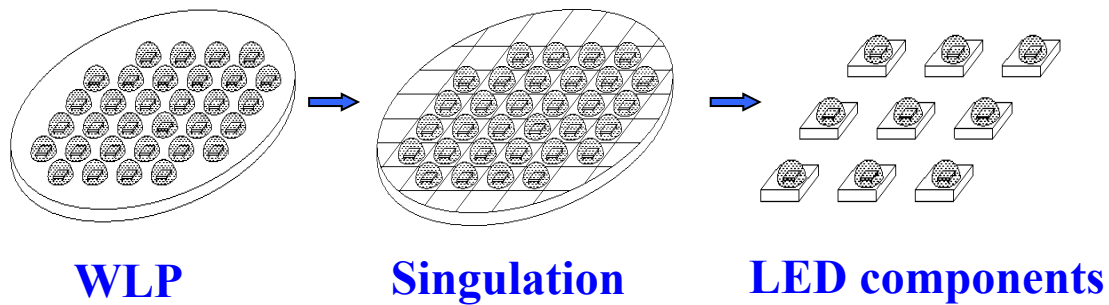
Laser Solder Ball Bumping



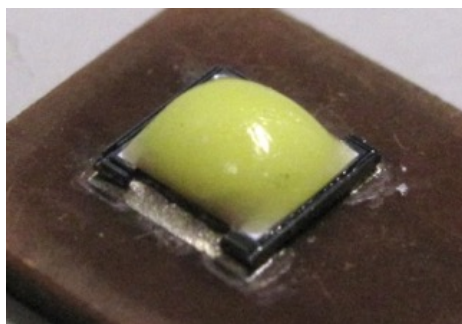
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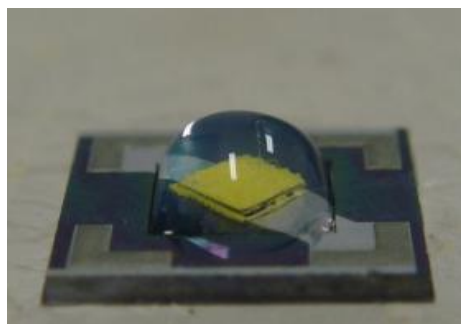
LED Wafer Level Packaging



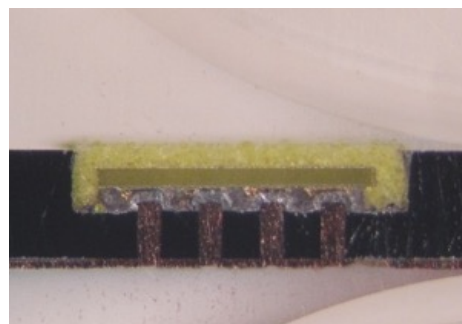
Silicon Carrier for LED WLP



WLP with Dispersed Phosphor



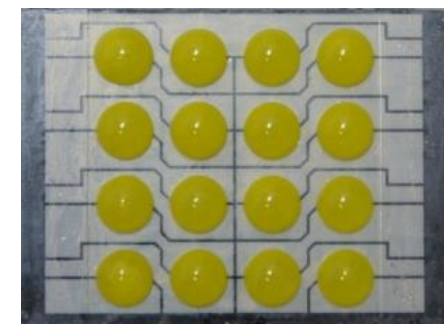
WLP with Conformal Phosphor by Mask Printing



WLP with Conformal Phosphor by Cavity Printing



WLP with Remote Phosphor Film



WLP with Remote Phosphor Cap

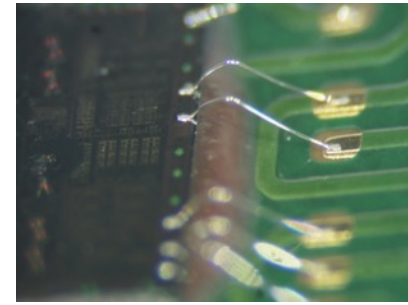


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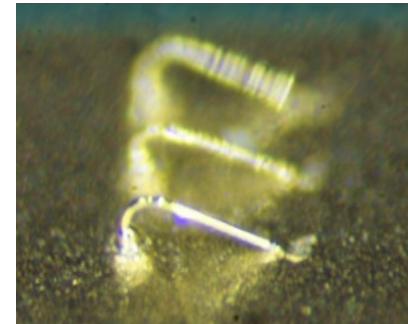


Wire Bonding

- ◆ Bond area:
 - Work holder: 6" x 4" (150mm x 100mm), max 200°C
 - Adjustable height: 0.625" (15.9mm)
 - Max bond span: 0.349" (8.9mm)
- ◆ Bond parameters:
 - Bond force: 10g-250g (low/high programmable)
 - Bond time: 0ms-999ms
 - Programmable: 40 device with 30 wire types, up to 5 bonds per wire, individual power, time and loop control data per wire type
 - Ultrasonics: 63kHz, 2.5W (4W optional)
- ◆ Wire capability:
 - Au/Al: 0.7 to 3mil (18 to 75µm)
 - Ribbon: 0.5x2mil to 1x10mil (12.5x50µm to 25x250µm)
 - Cu ball bonding: 0.7 to 1.5mil (18 to 38µm)



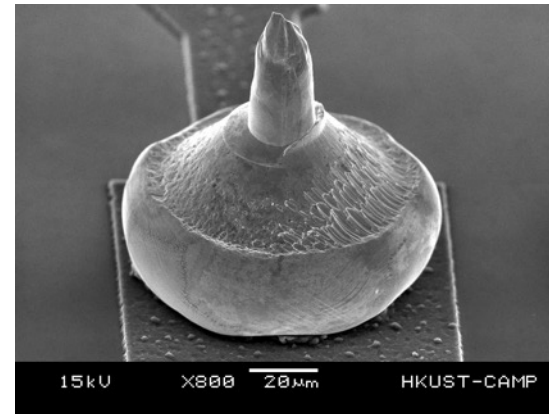
Al Wire



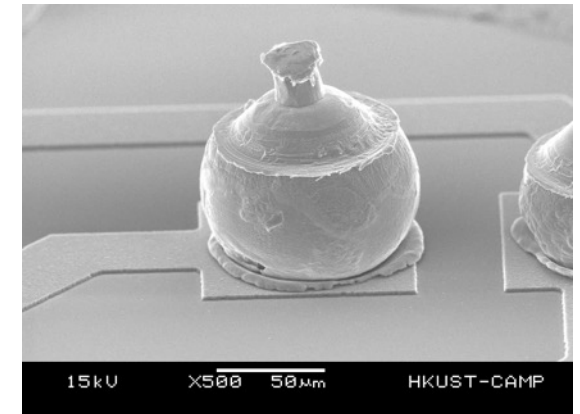
Gold Wire



4KE Convertibility Semi-Automatic Wire Bonder



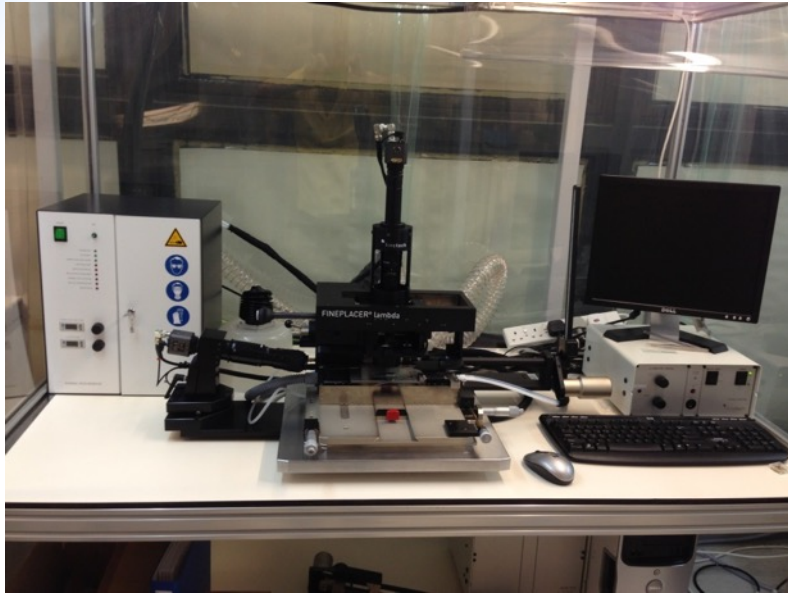
Gold Stud



Copper Stud

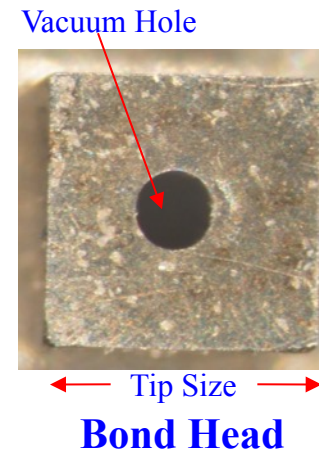
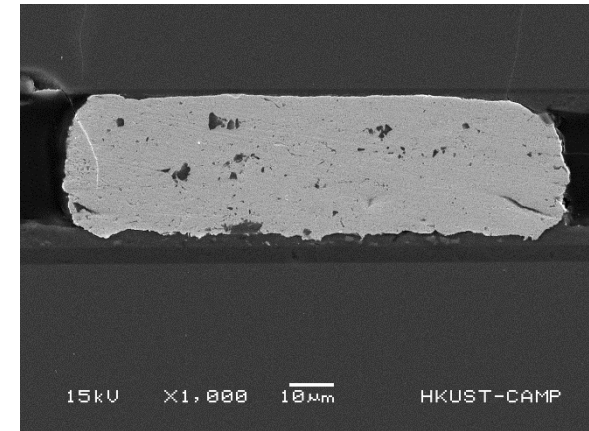
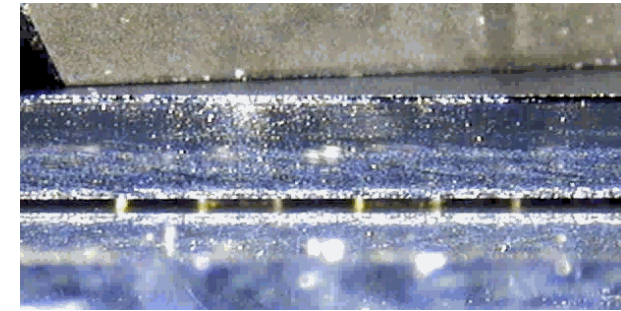


Flip Chip Bonding



Fine Tech Flip Chip Bonder

- Bonding Accuracy: 0.5 μm
- Max. Die/Package Size: 16 mm (Pick-n-Place Only)
- Substrate Size
 - 50 x 50 mm (Thermal Compression)
 - 180 x 108 mm (Pick-n-Place only)
- Bonding Environment
 - Nitrogen / Formic Acid
- Bonding Mechanism
 - Thermal compression (Bond Force 0.1 – 200 N)
 - Reflow (RT-400°C, Heating Rate: 20°C/s)
 - Thermosonic



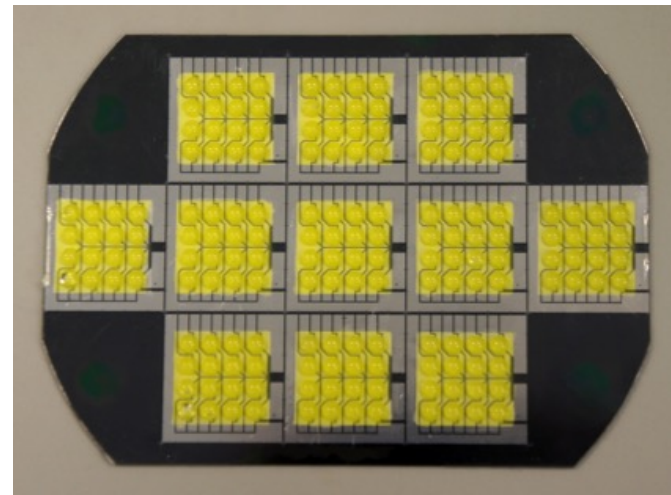
Bonding Mechanism	Thermal Compression					Thermosonic		
	1	2	3	4	5	1	2	3
Tip Size, mm	0.5	1	3	5	10	0.5	1	3
Vacuum Hole Size, mm (Min. Die Size)	0.15	0.3	0.6	2	4	0.12	0.3	0.65



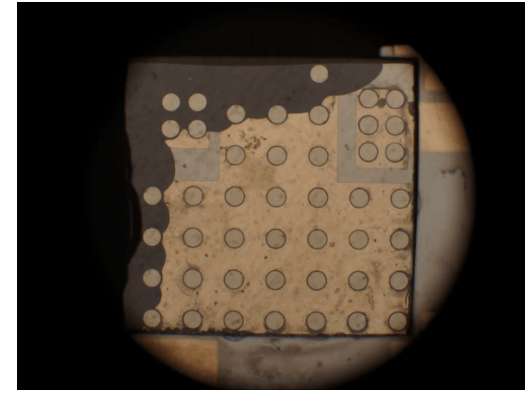
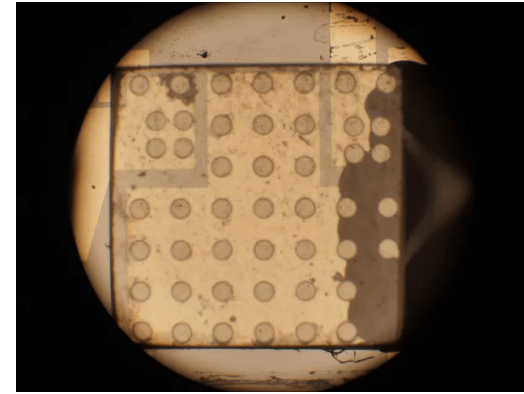
Molding and Underfill Encapsulation



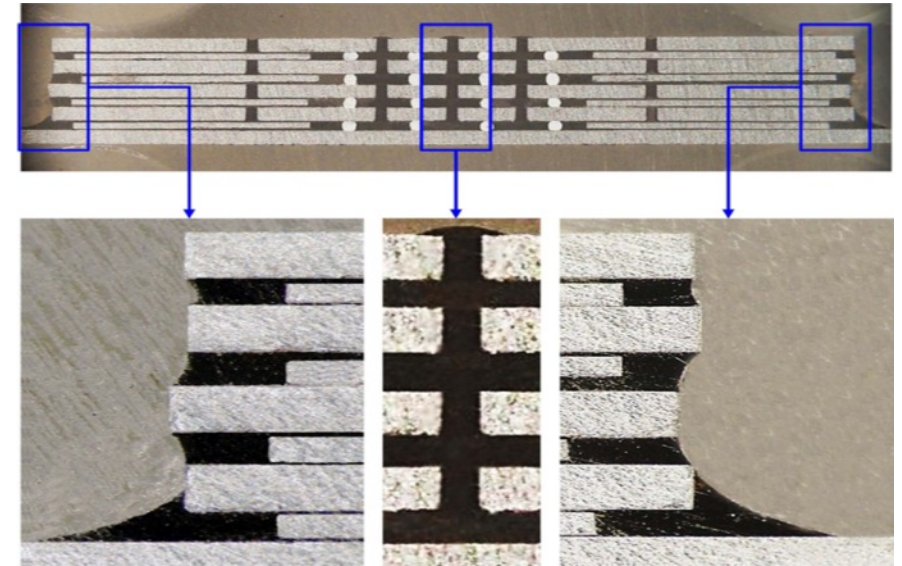
Transfer Molding



Compression Molding for LED WLP



Underfill Dispensing



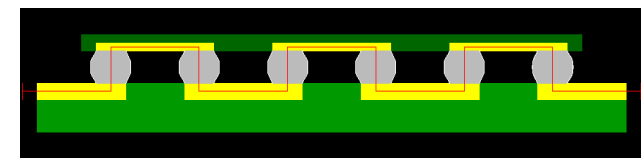
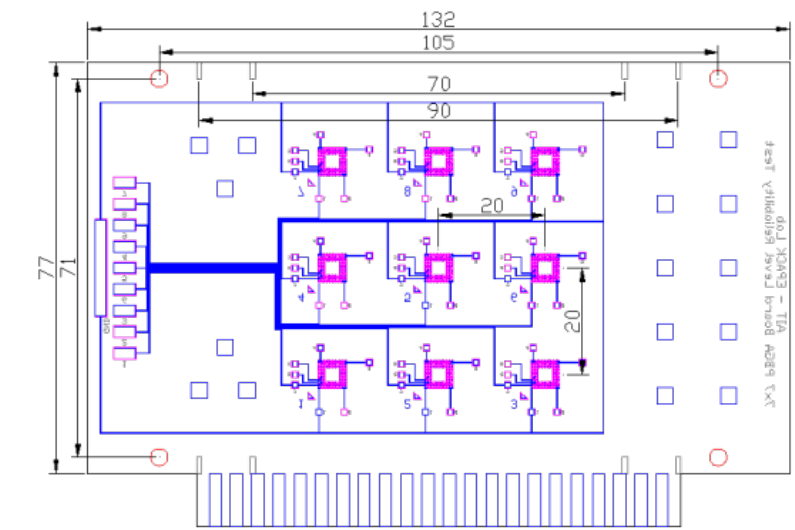
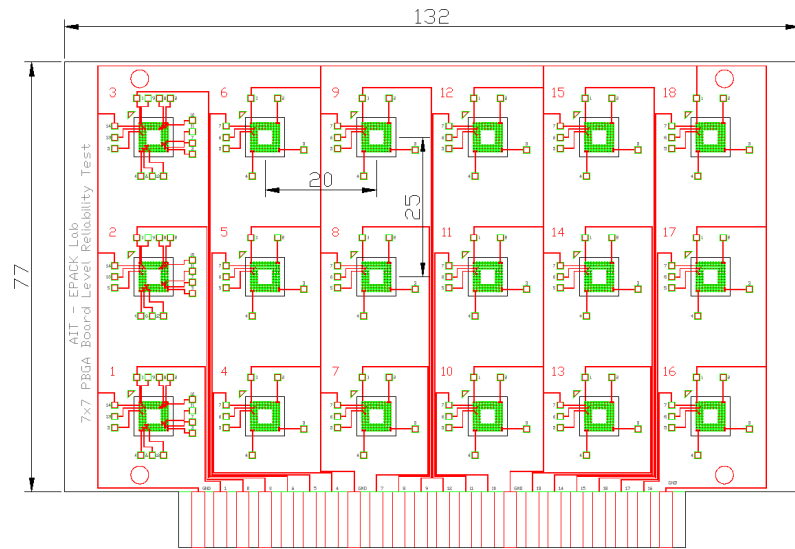
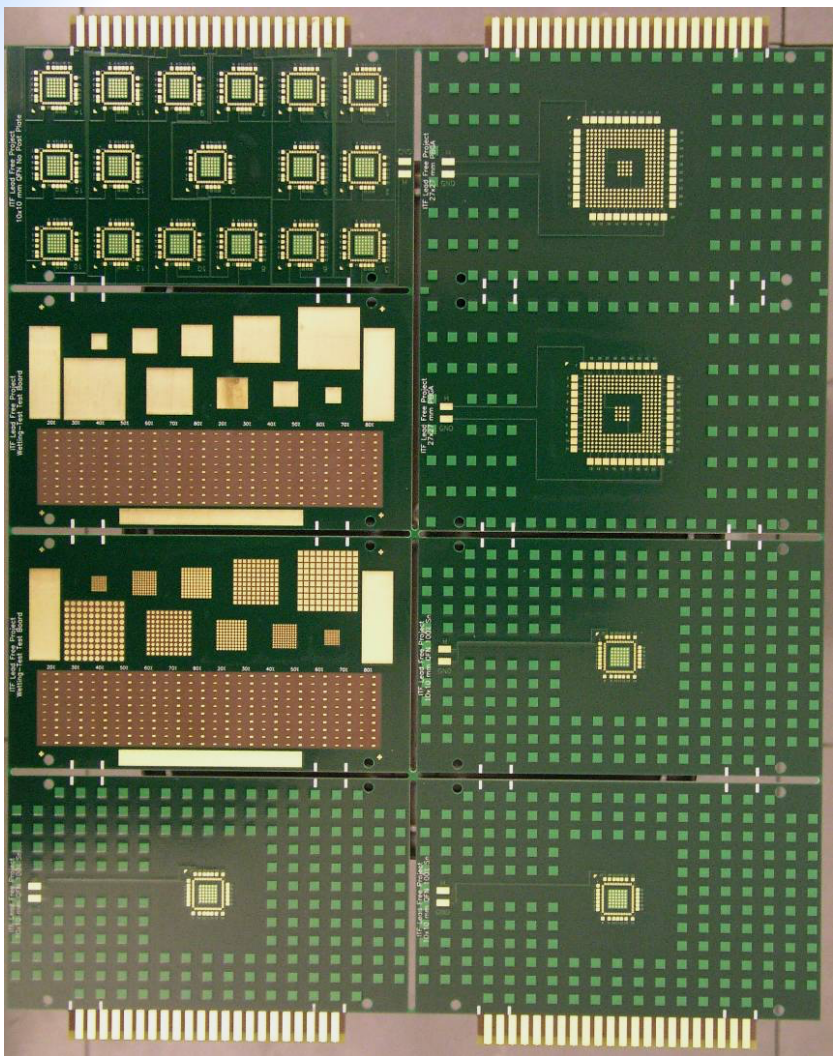
Underfill Encapsulation for 3D Package



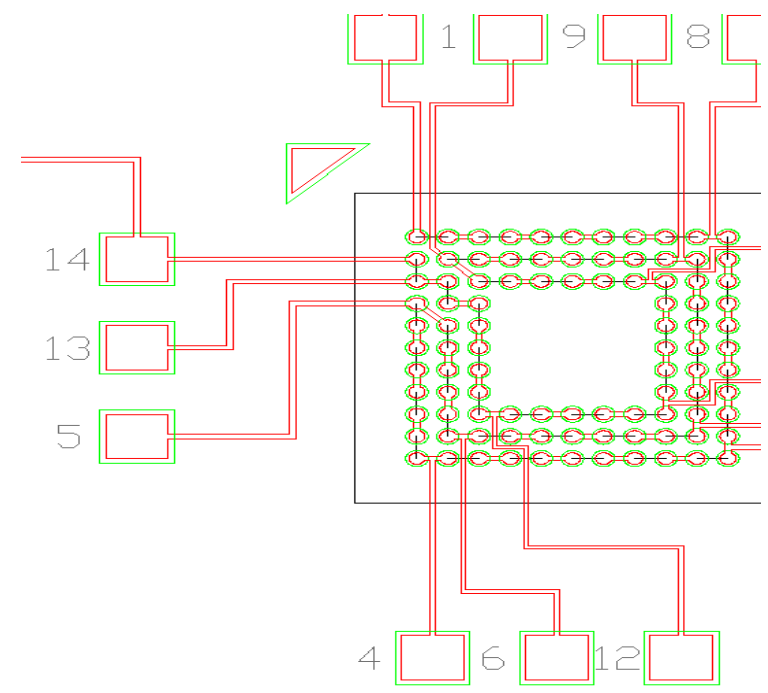
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PCB Layout Design for Reliability Tests



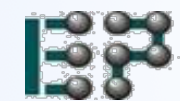
Mechanism of Daisy Chain



Daisy Chain Design with Local Probing



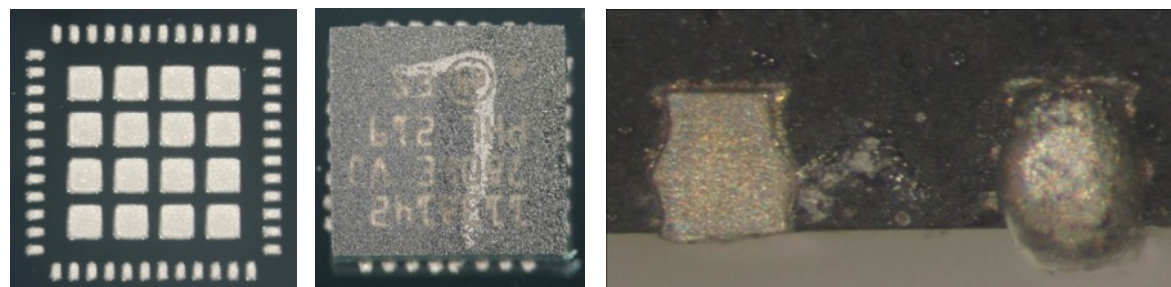
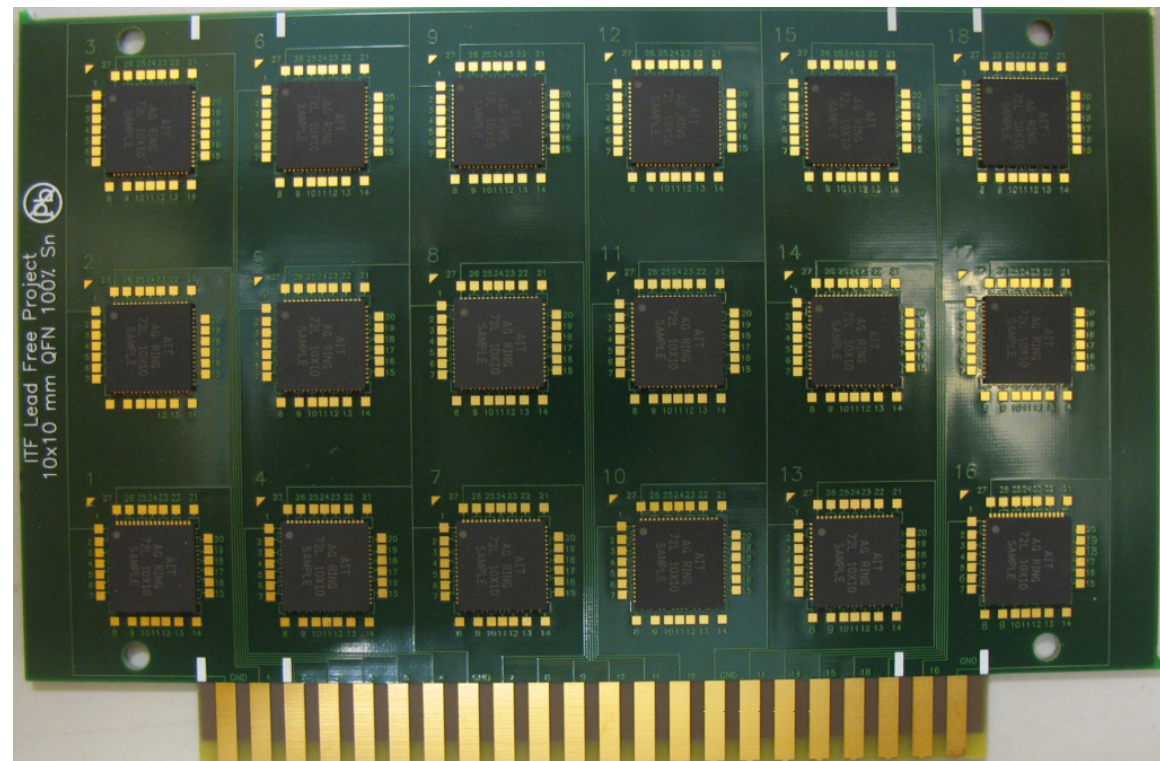
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SMT and Solderability Test



8 Zones Reflow Oven

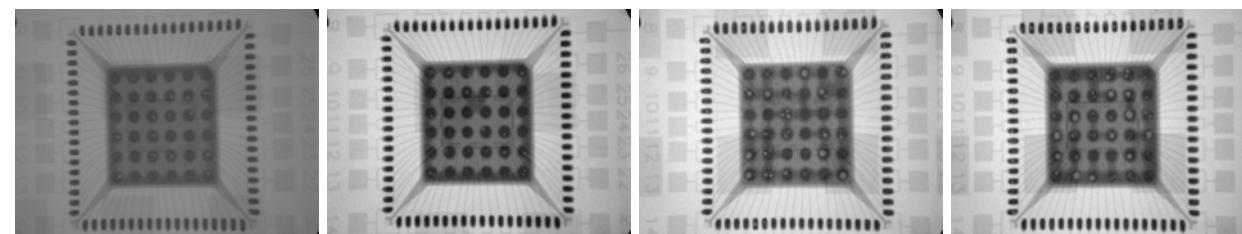


Paste Printing

Pick-n-Place

Wettability Inspection

Solderability Test



SAC305

SAC387

SCN

SACC



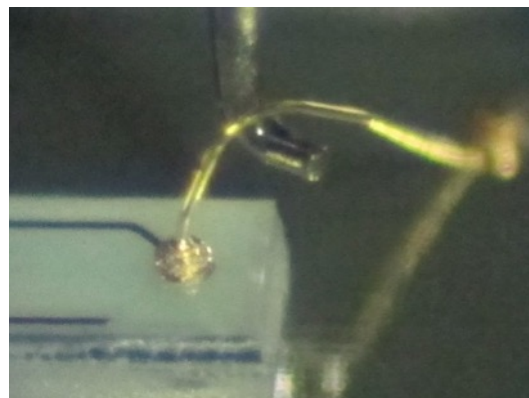
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Package Level Reliability Tests



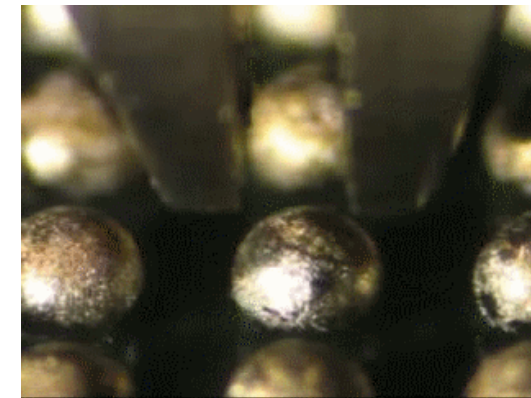
DAGE 4000 Plus Microtester



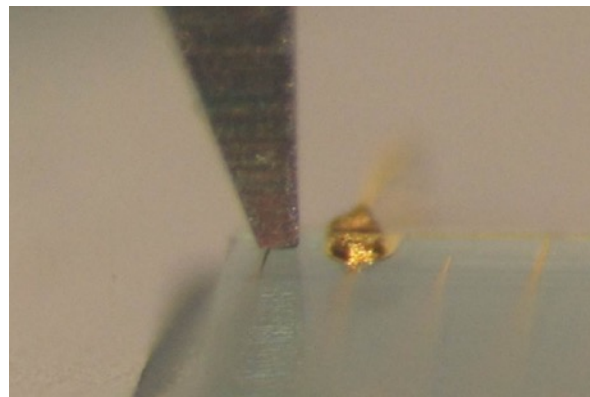
Wire Pull



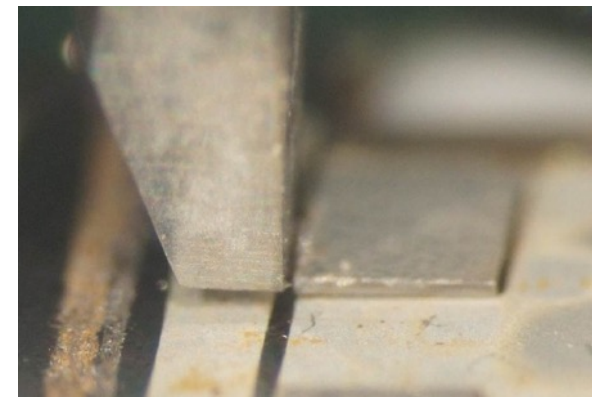
Button Shear



Solder Ball Pull



Bump Shear



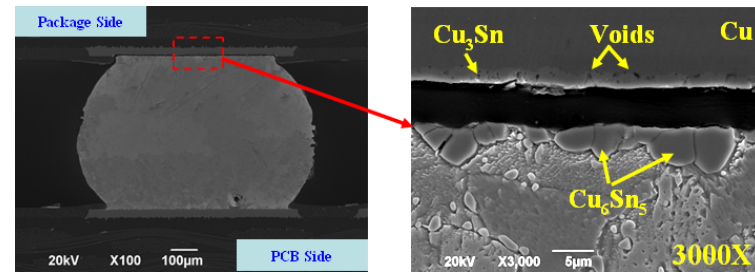
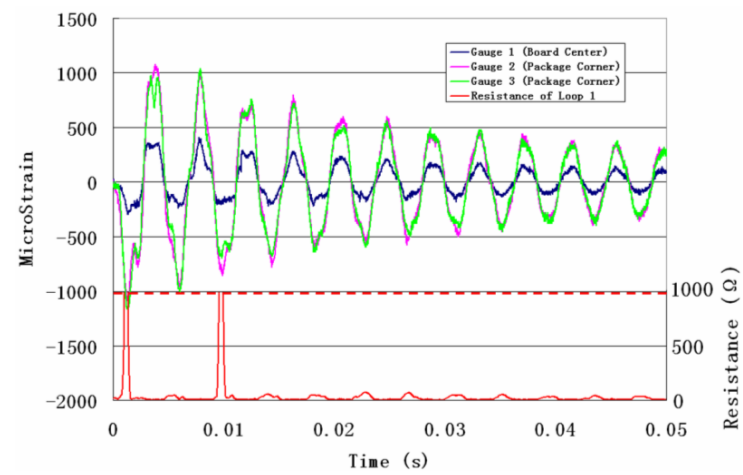
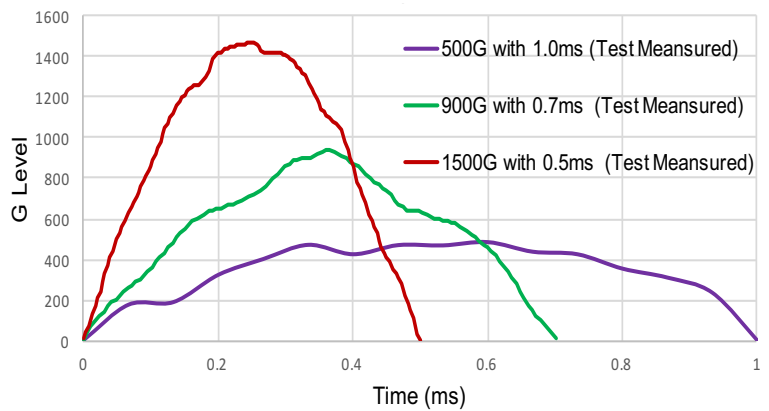
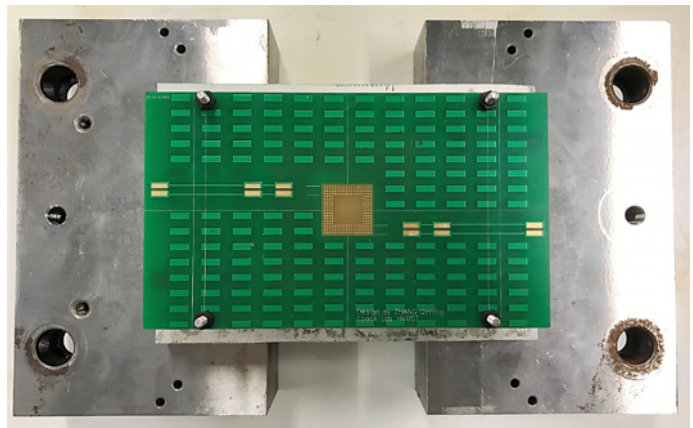
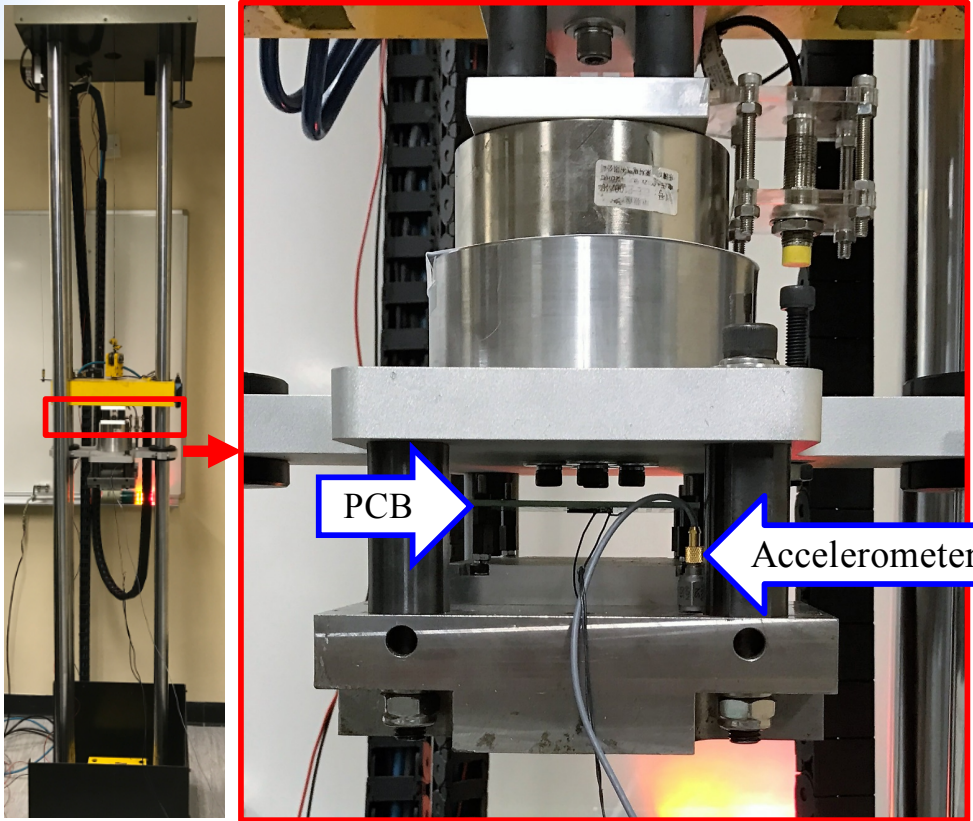
Die Shear



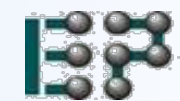
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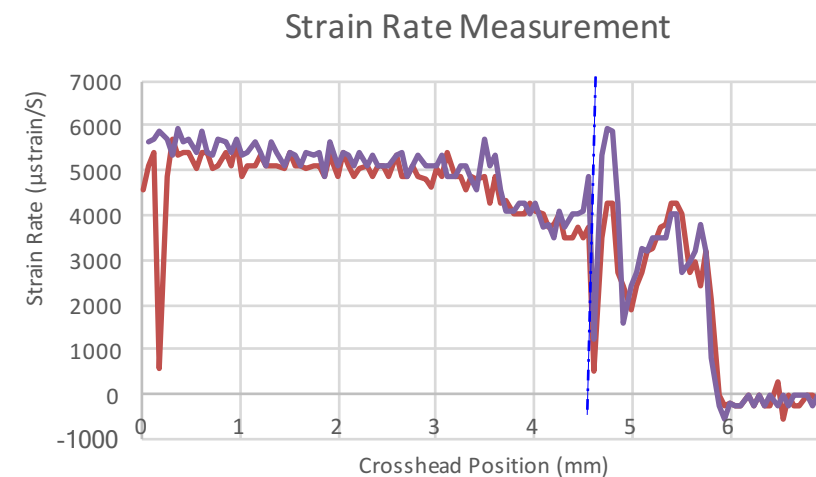
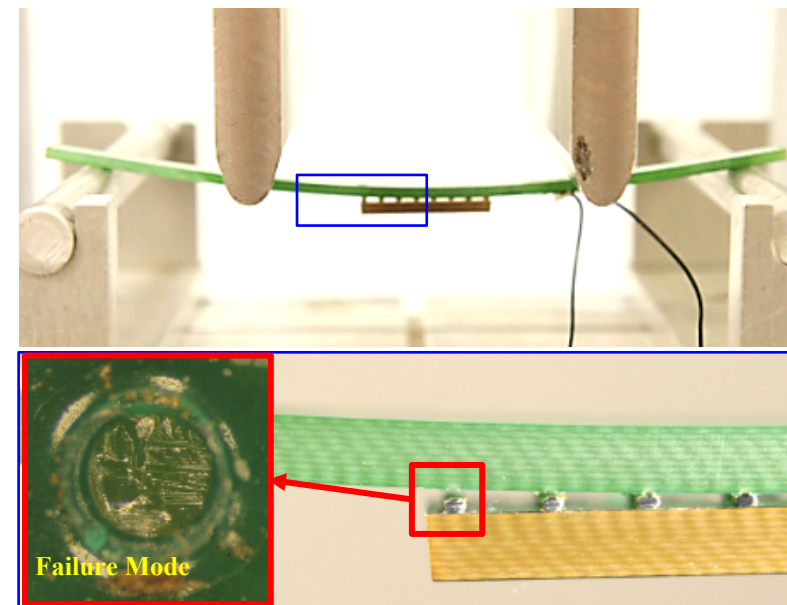
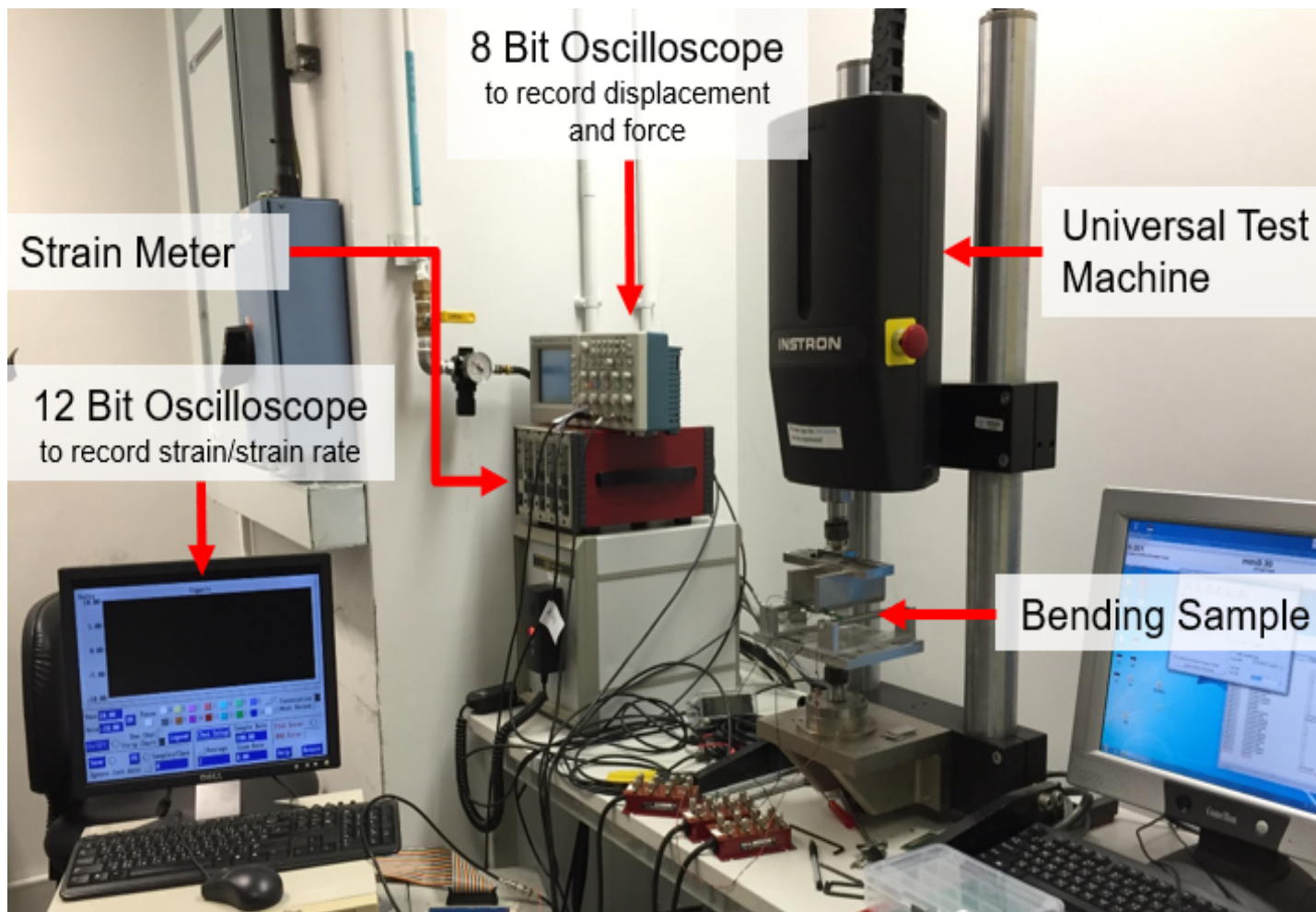
Board Level Reliability Test



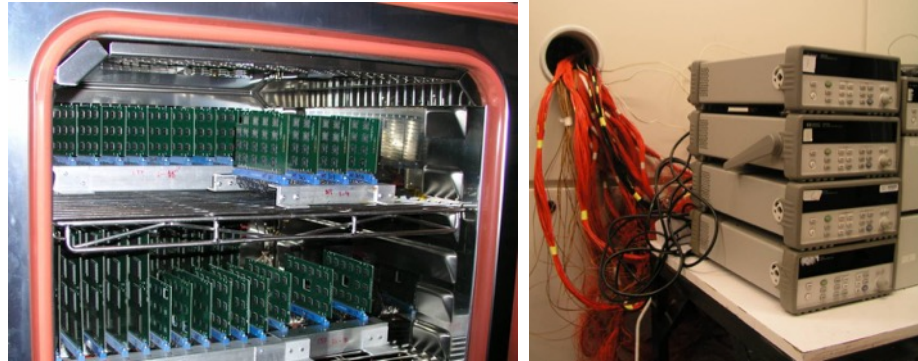
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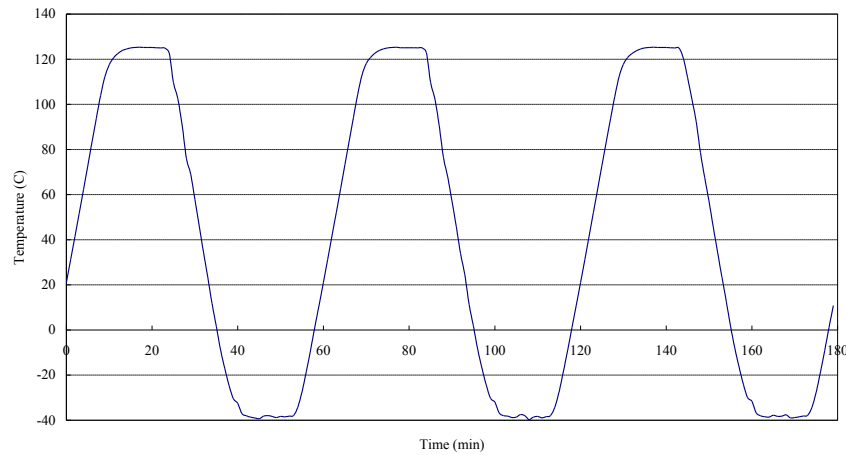
Board Level Reliability Test (Bending)



Board Level Reliability Test (ATC)

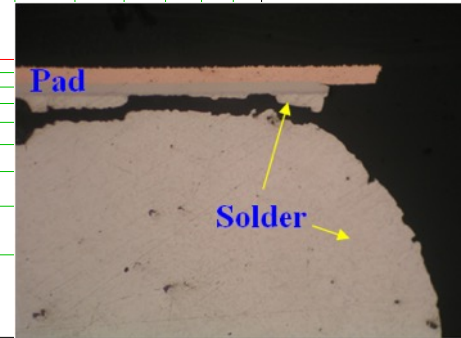
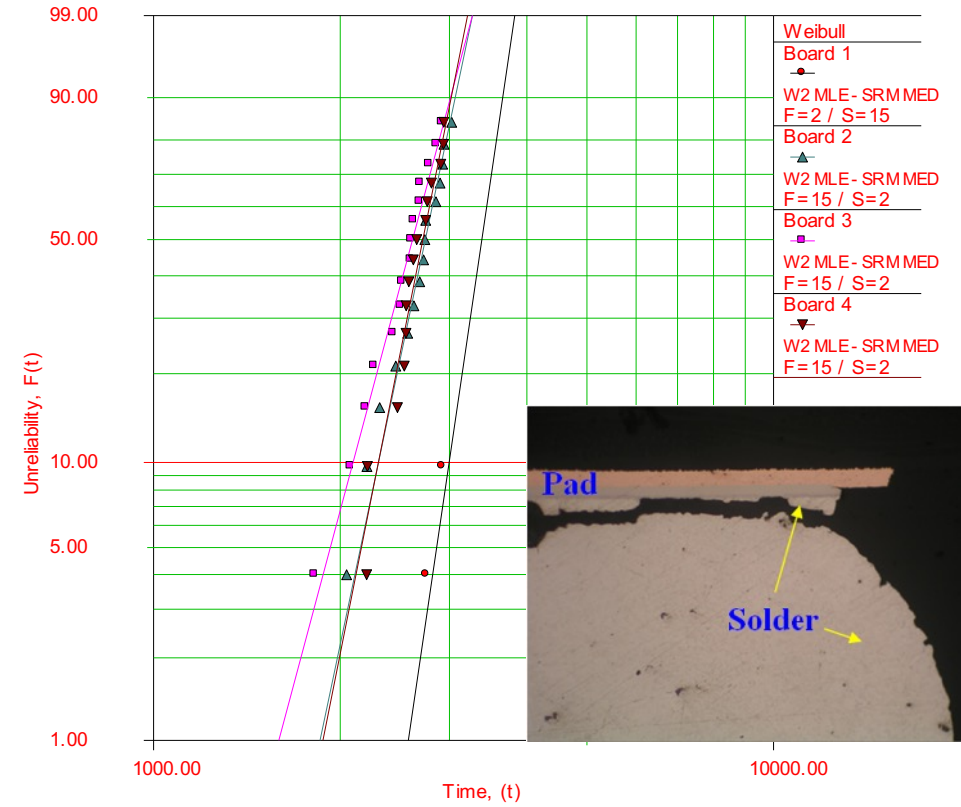


Thermal Cycling Profile



ReliaSoft's Weibull++ 6.0 - www.Weibull.com

Probability - Weibull



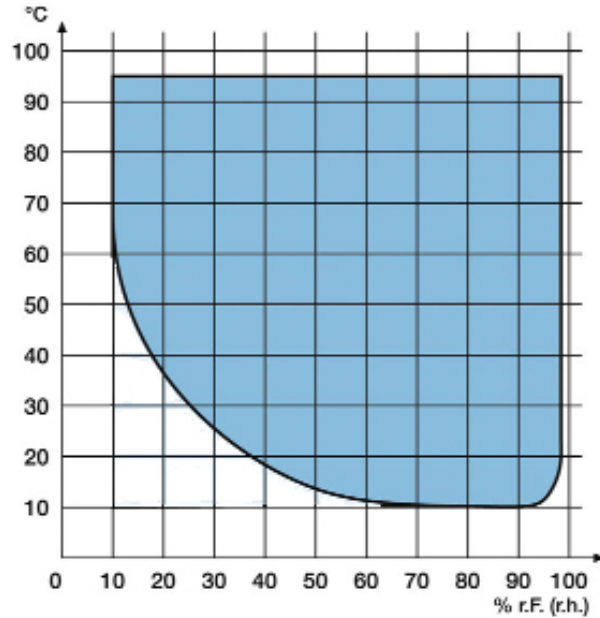
$\beta_1=15.4986, \eta_1=3466.5616$
 $\beta_2=10.8255, \eta_2=2838.8649$
 $\beta_3=8.5213, \eta_3=2731.6031$
 $\beta_4=11.4088, \eta_4=2807.5367$



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Environmental Chambers



Humidity Chamber

- Chamber size: W350 × D300 × H310 mm
- Maximum temperature: 180 °C
- Minimum temperature: -40 °C
- Maximum ramp up rate: 4 °C/min
- Maximum ramp down rate: 6 °C/min



HAST

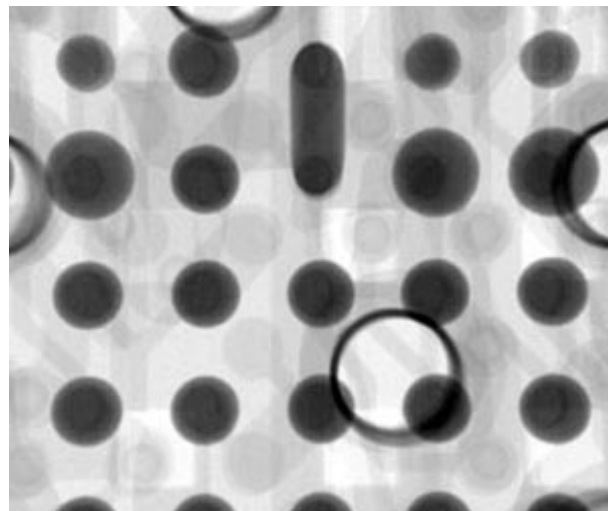
- Interior dimension: 350 mm × 430 mm × 350 mm
- Temperature range: 105.0 ~ 142.9 °C
- Humidity range: 75% ~ 100% RH
- Pressure: 0.02 ~ 0.196 MPa



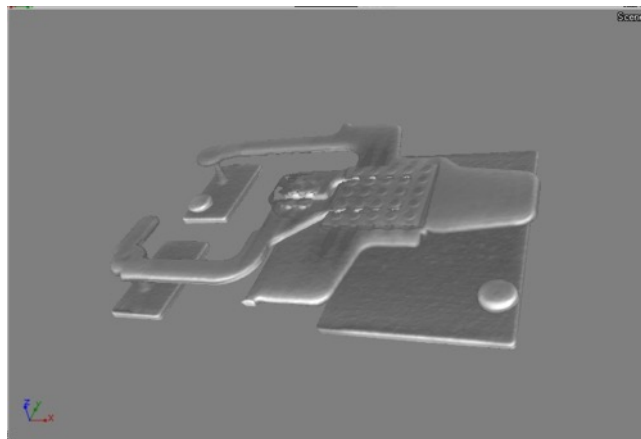
Failure Analysis (Non-Destructive)



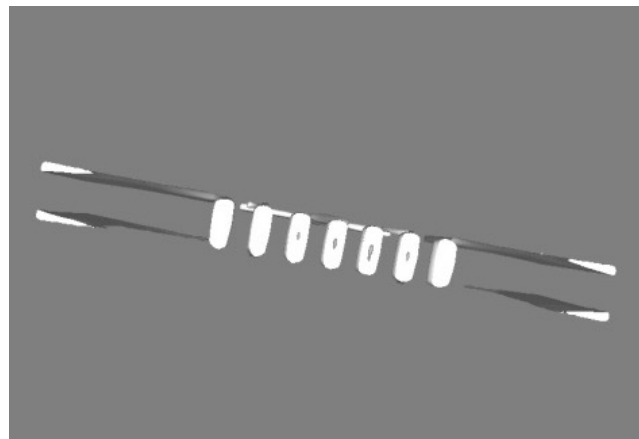
X-RAY



2D X-Ray



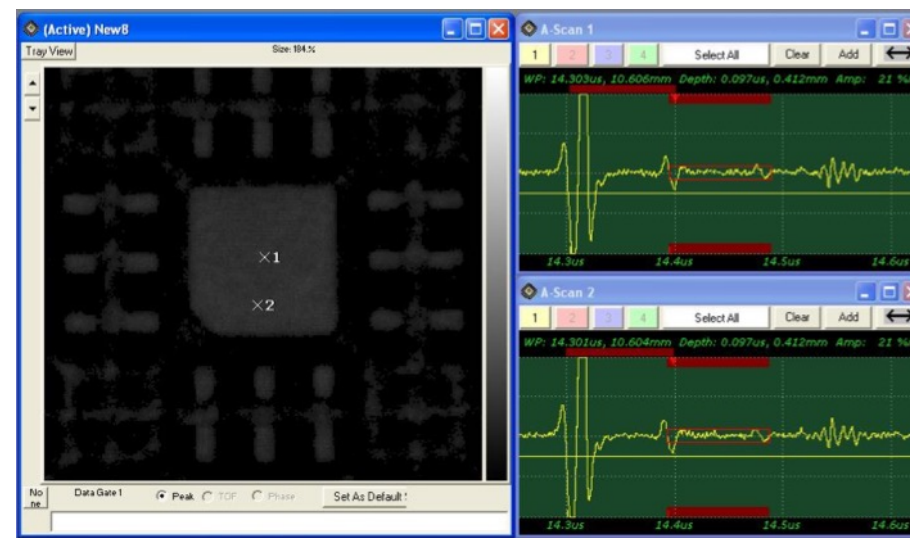
3D X-Ray



3D X-Ray Cross-Section



Scanning Acoustic Microscopy (SAM)



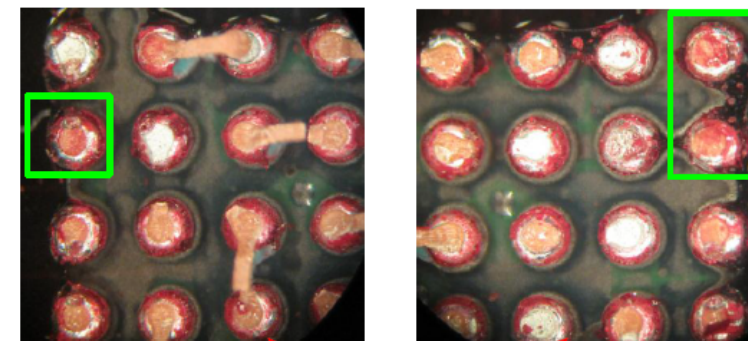
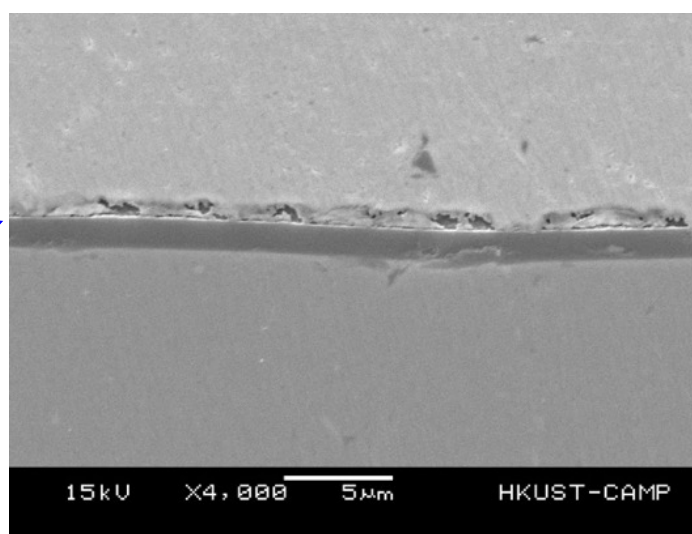
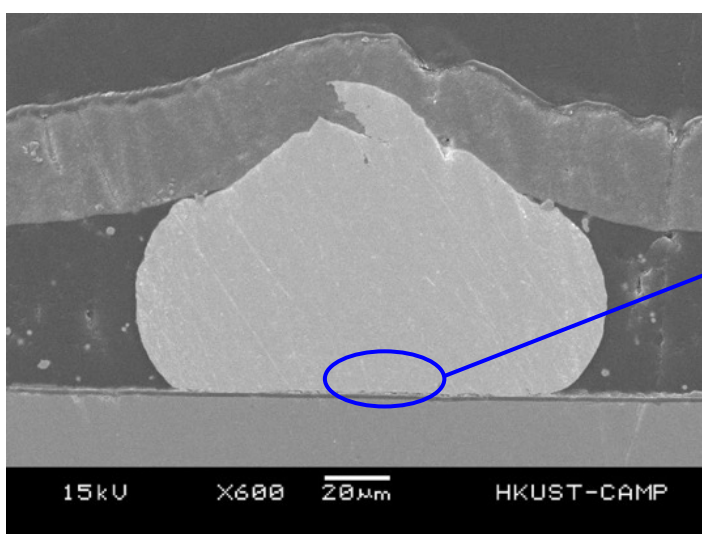
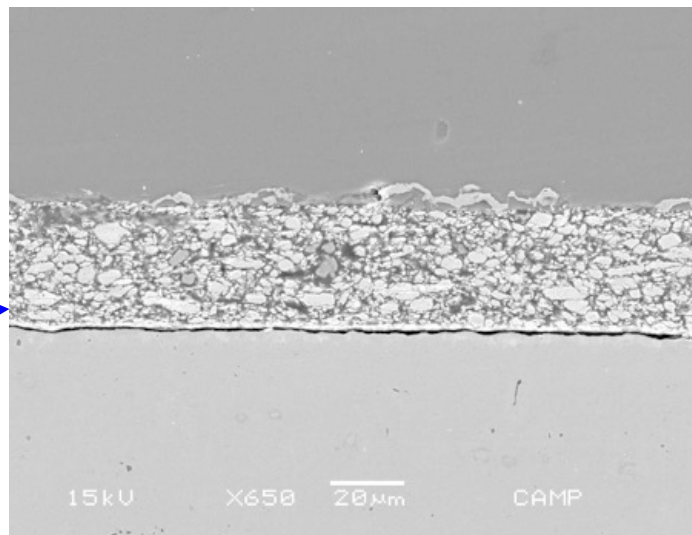
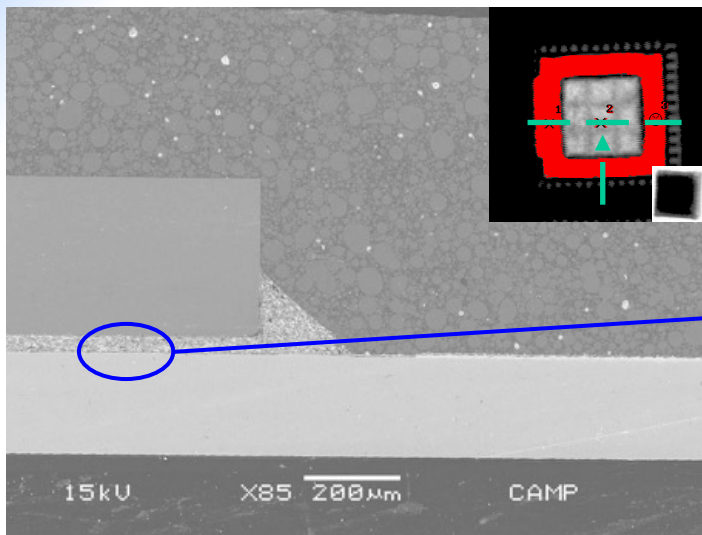
A-Scan & C-Scan



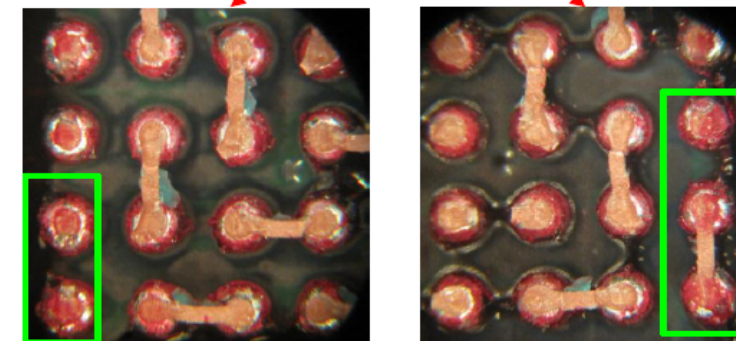
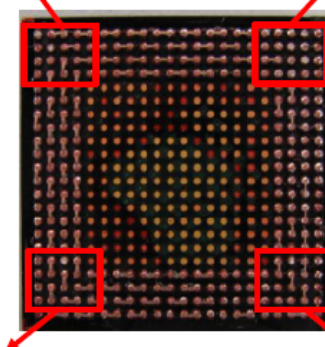
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Failure Analysis (Cross-Section and Dye Penetration)



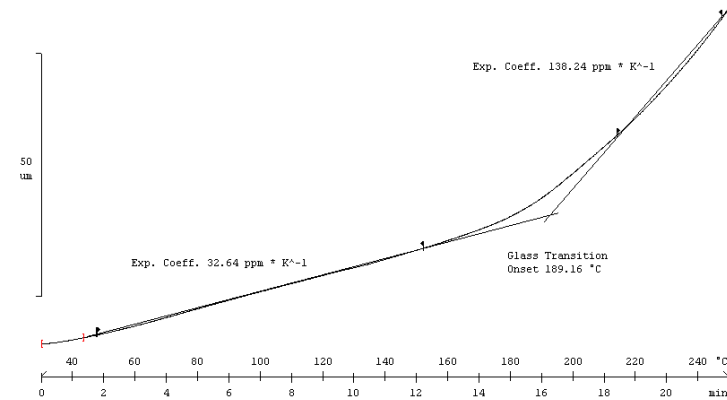
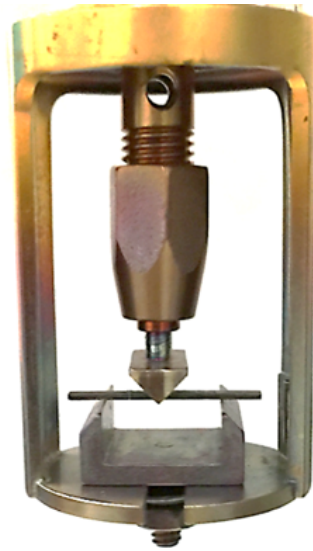
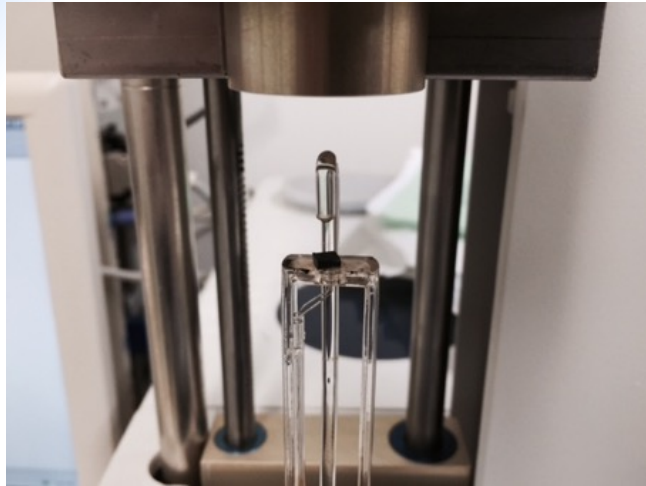
Package



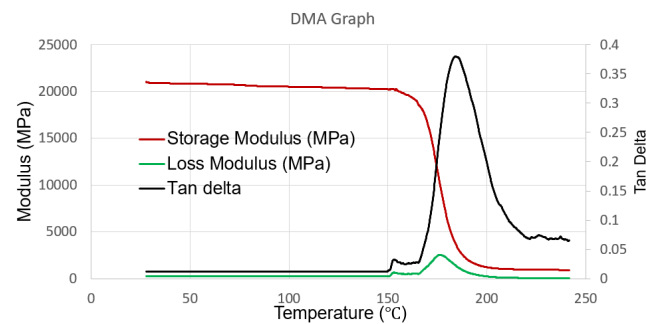
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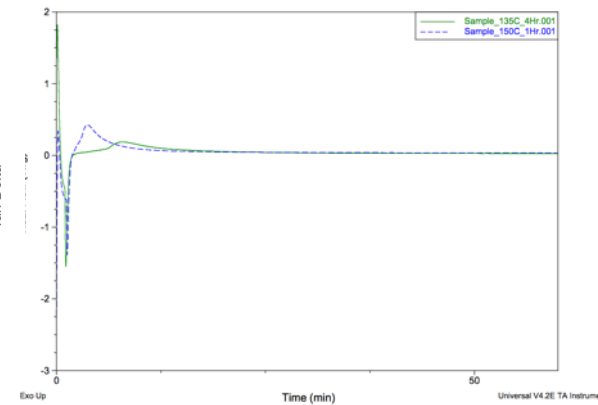
Material Characterizations (Thermal Analysis)



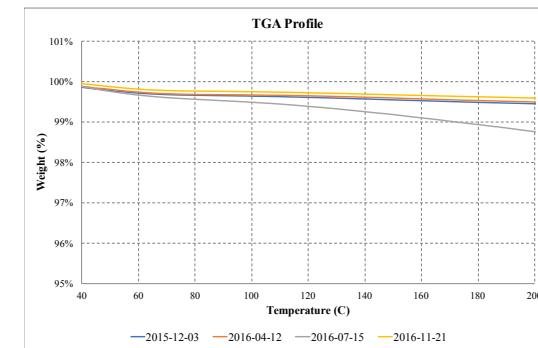
TMA



DMA



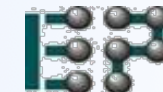
DSC



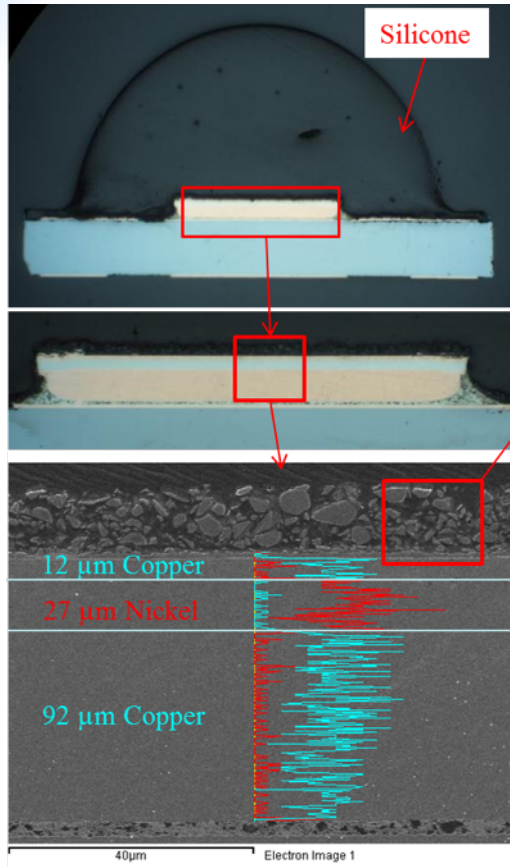
TGA



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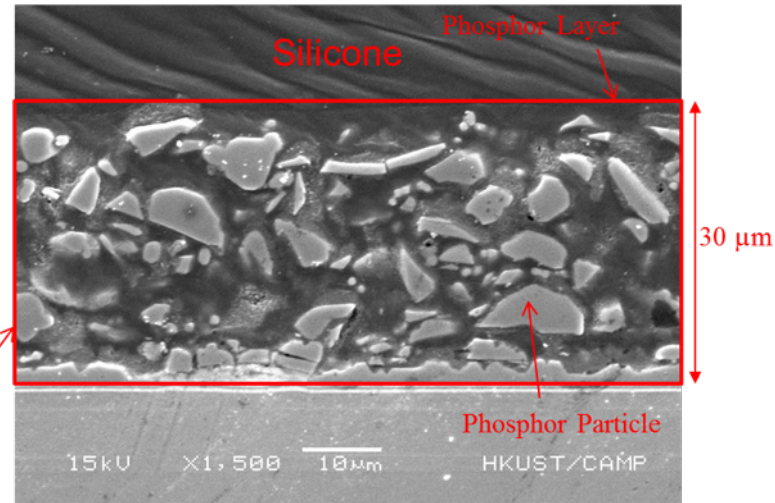


Material Characterizations

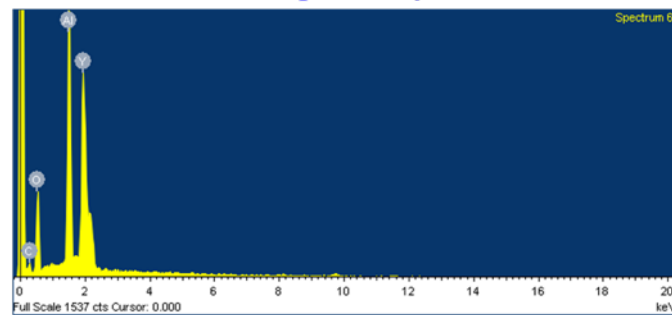


LED Chip

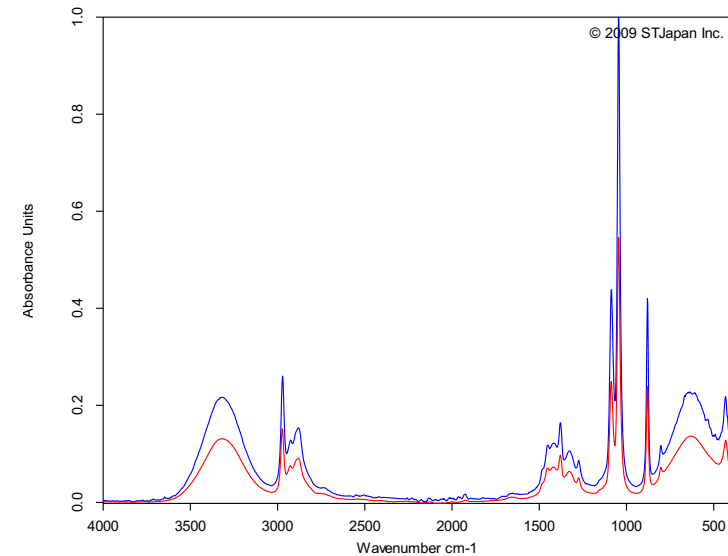
SEM/EDX Inspection



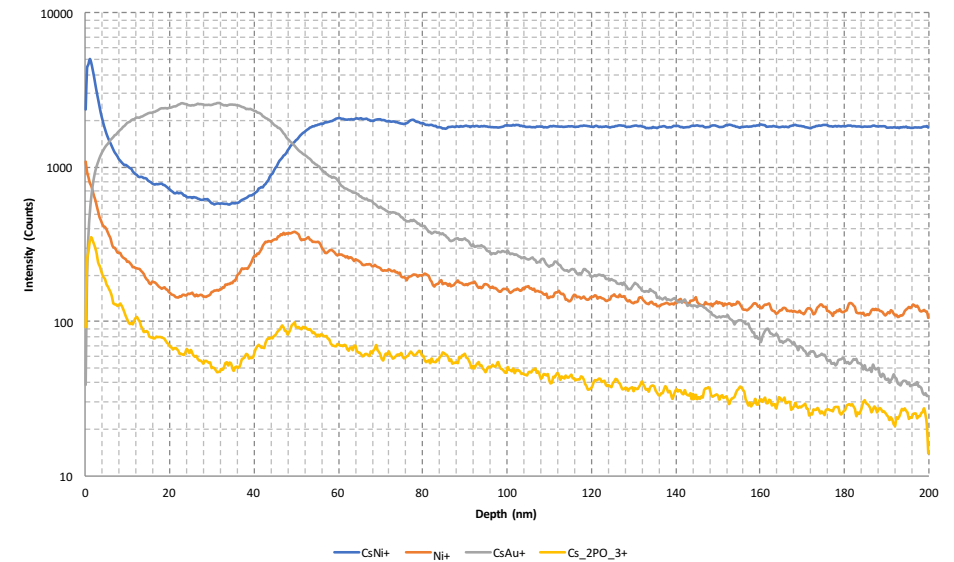
Phosphor Layer



Phosphor Particle (Yttrium + Aluminum)



FTIR



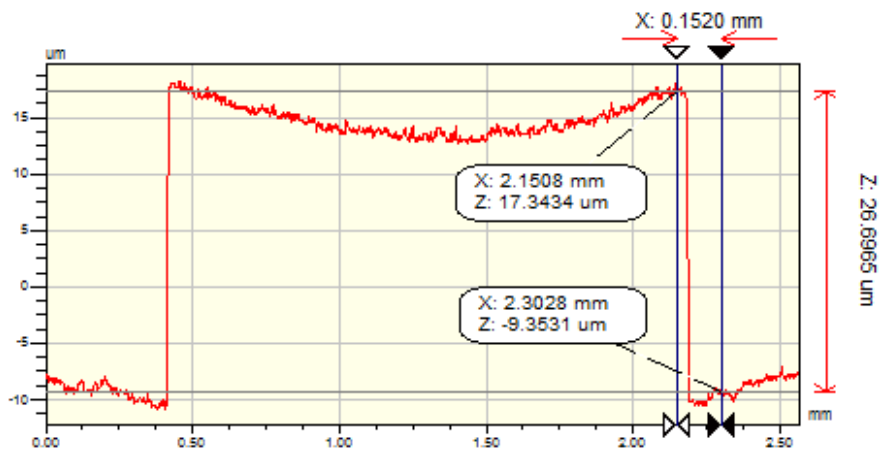
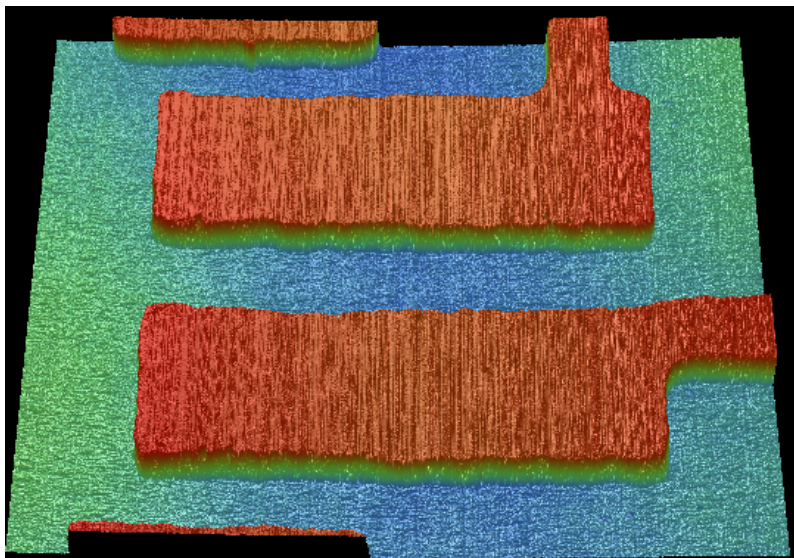
SIMS Depth Profile



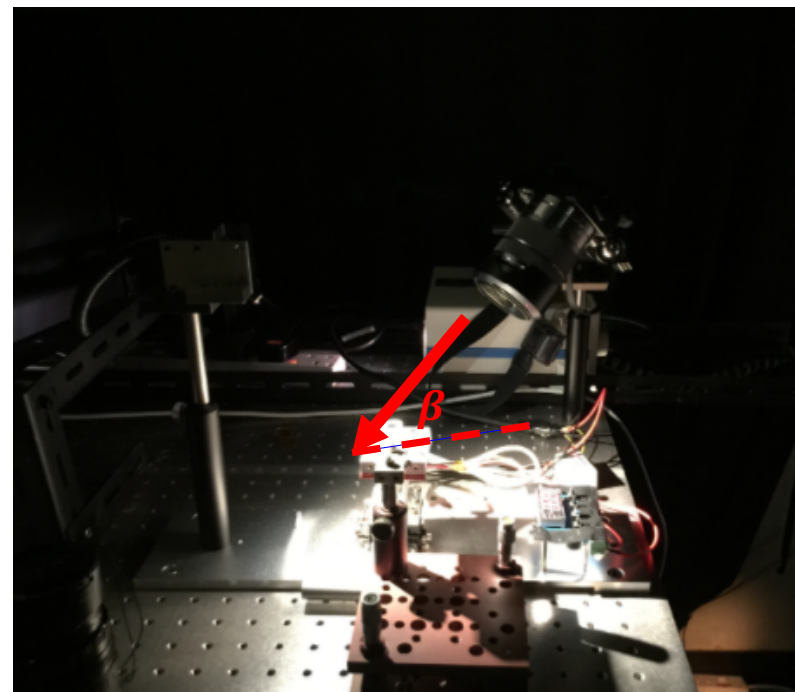
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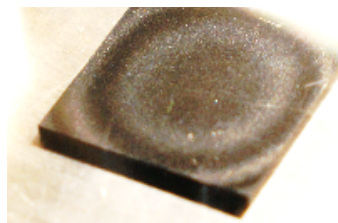
Roughness and Warpage Inspection



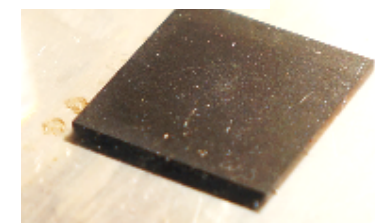
Surface Profiler



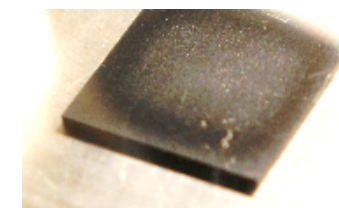
100°C $w = -50\mu\text{m}$



175°C $w = 0\mu\text{m}$



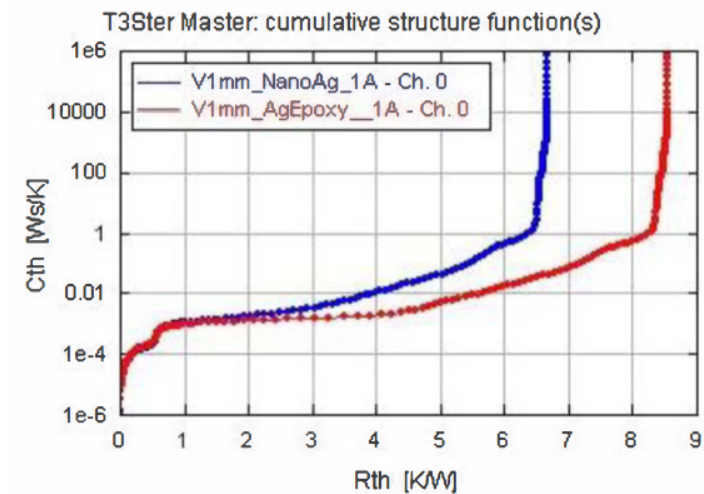
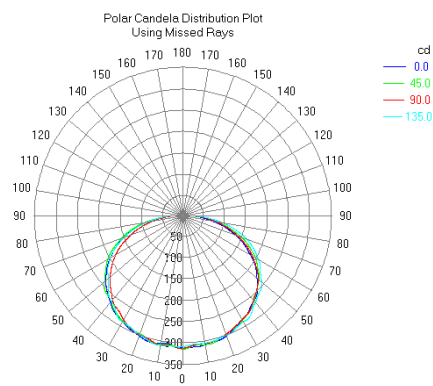
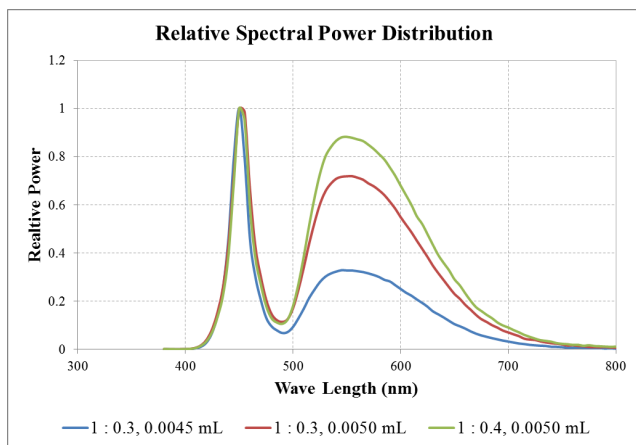
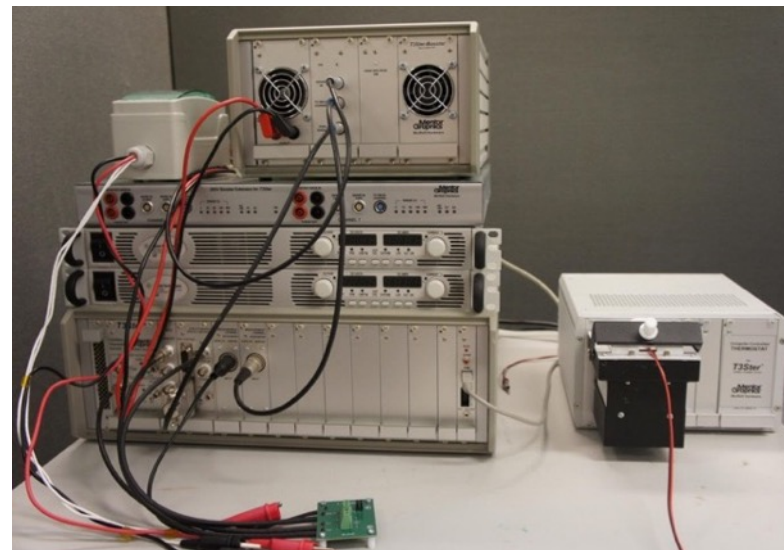
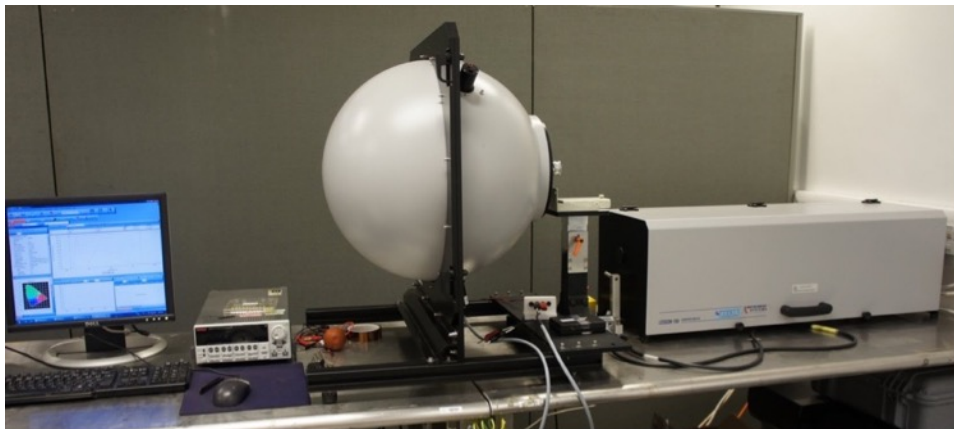
200°C $w = 30\mu\text{m}$



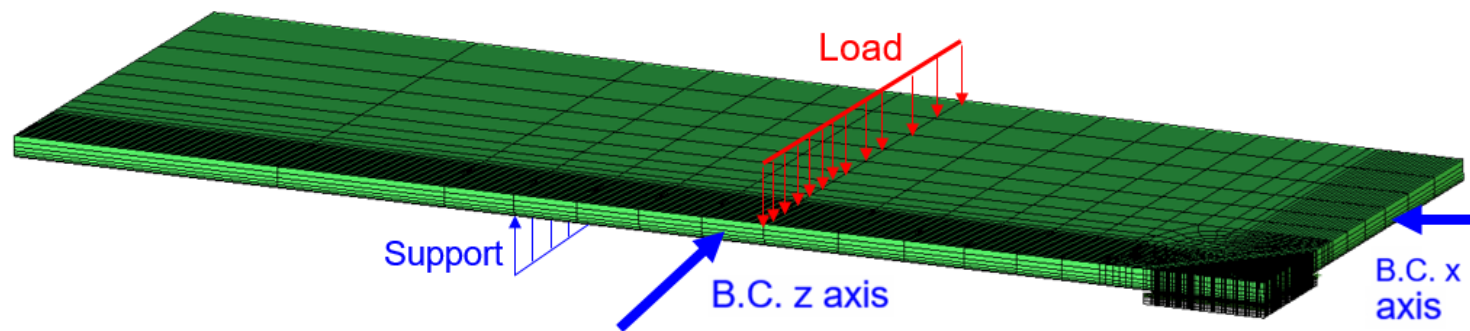
Shadow Morrie



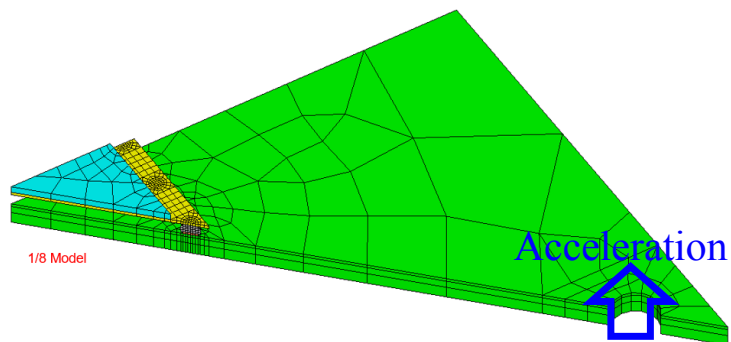
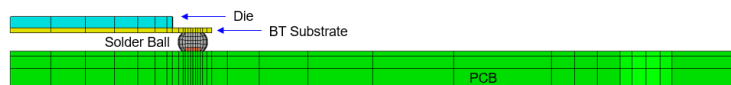
Optical and Thermal Characterizations



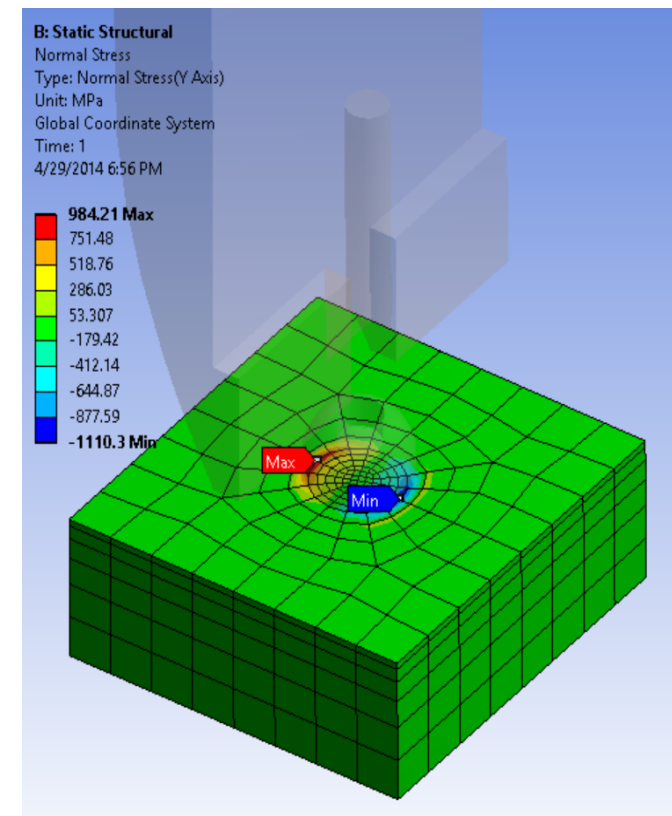
Mechanical Simulation



Monotonic/Cyclic Bending



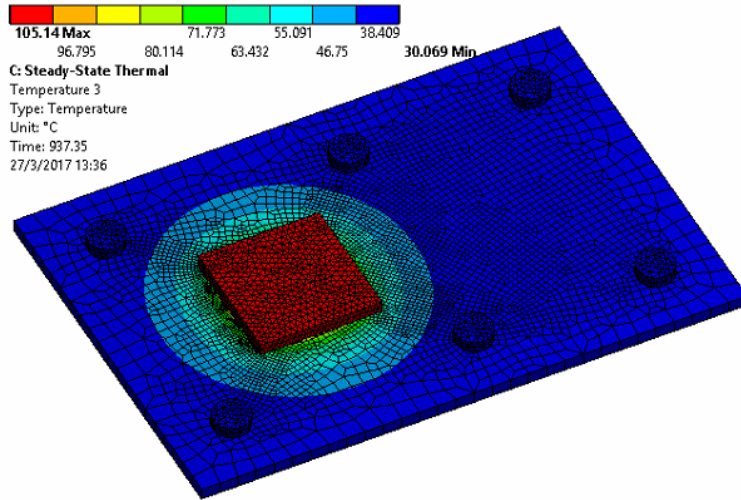
Board Level Drop



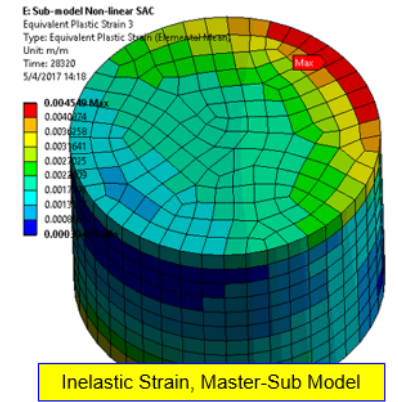
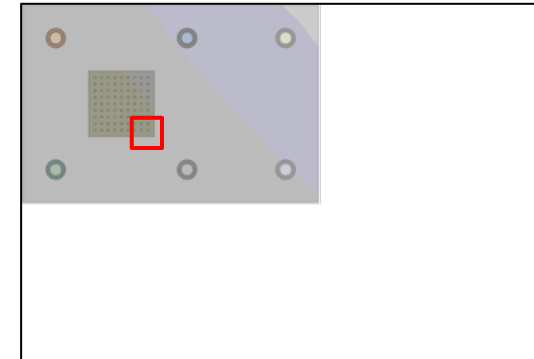
Pin Pull/Shear



Thermo-Mechanical Simulation

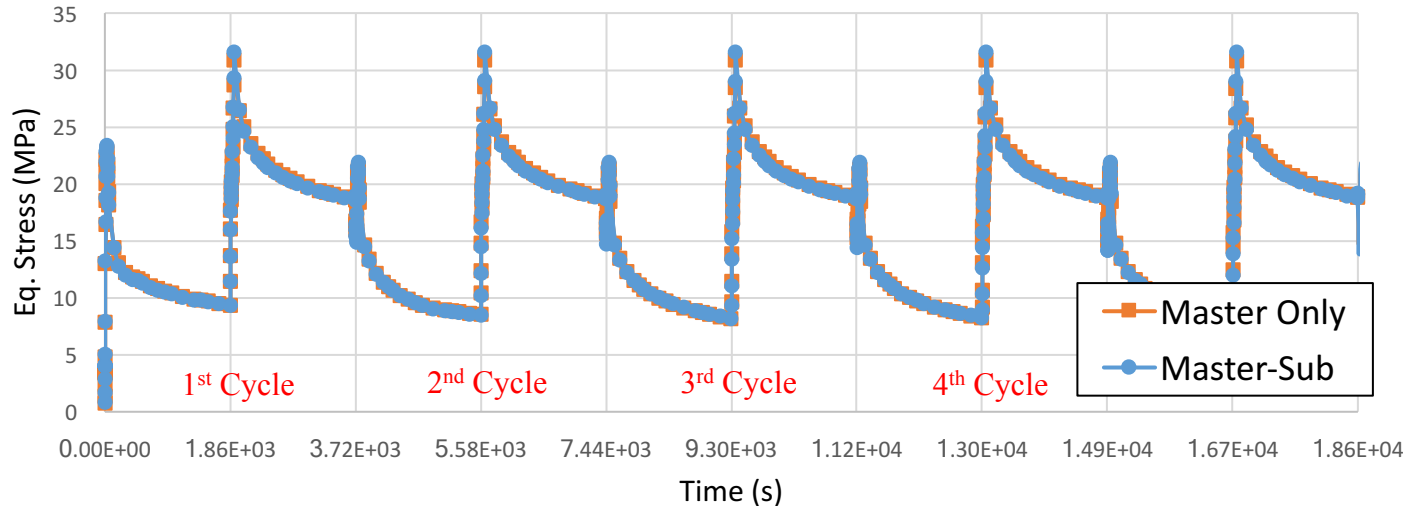


Temperature Distribution under Power Cycling

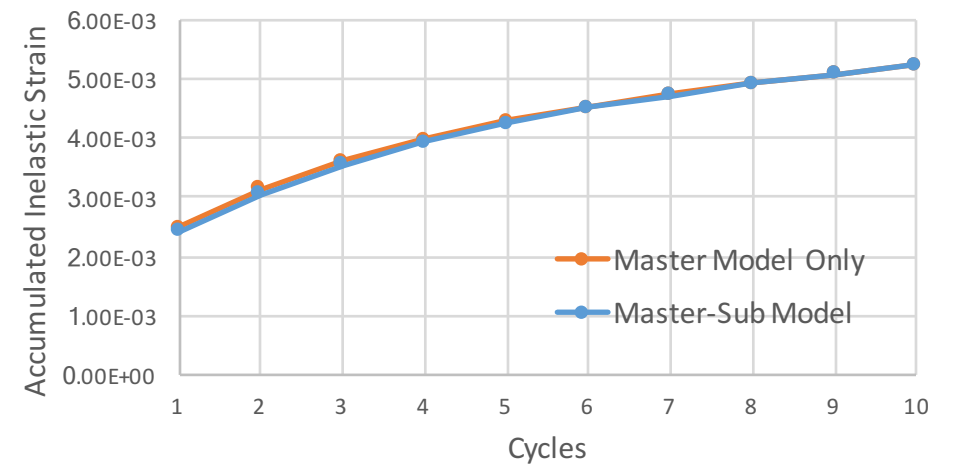


Inelastic Strain on Solder Bump

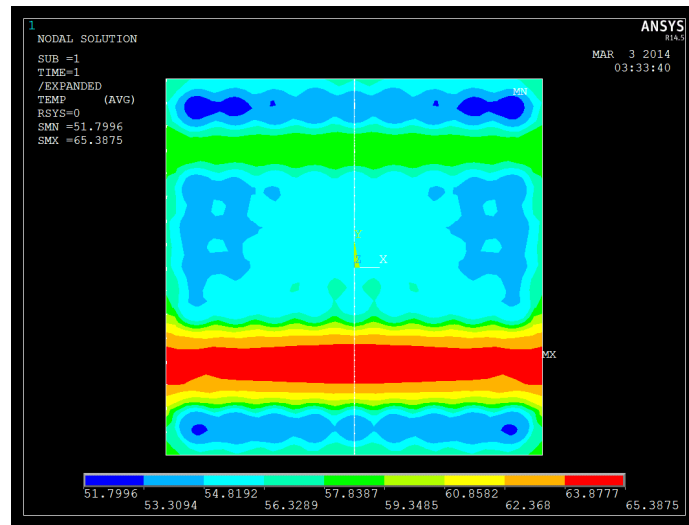
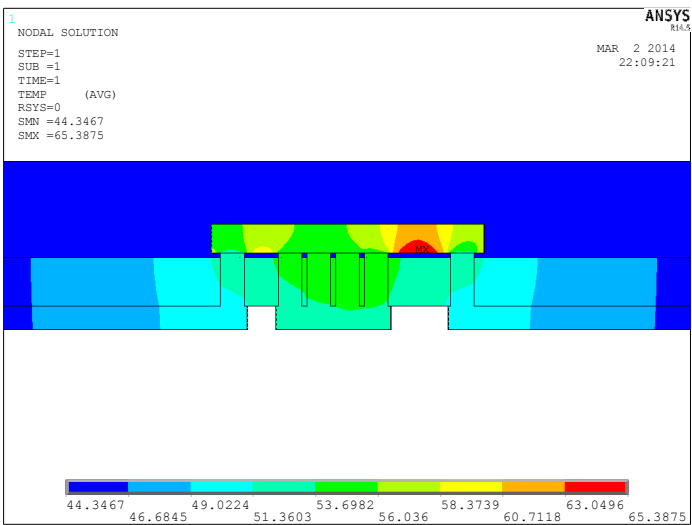
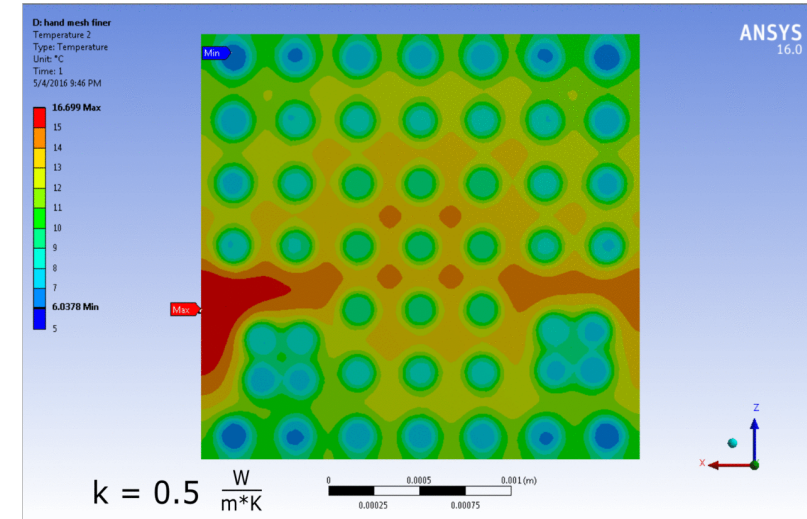
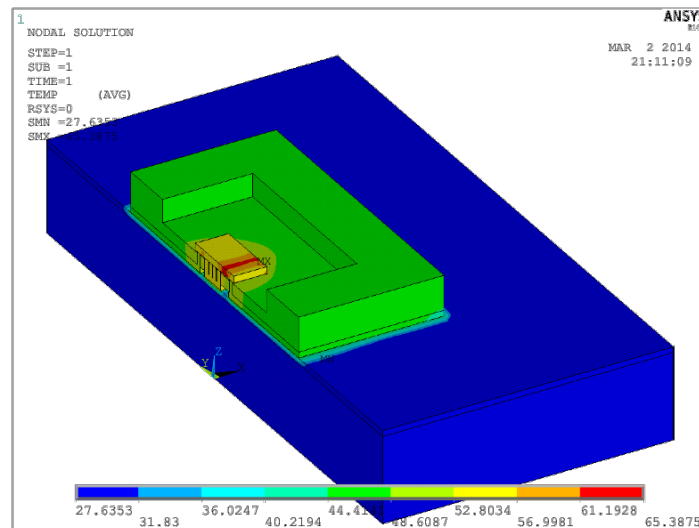
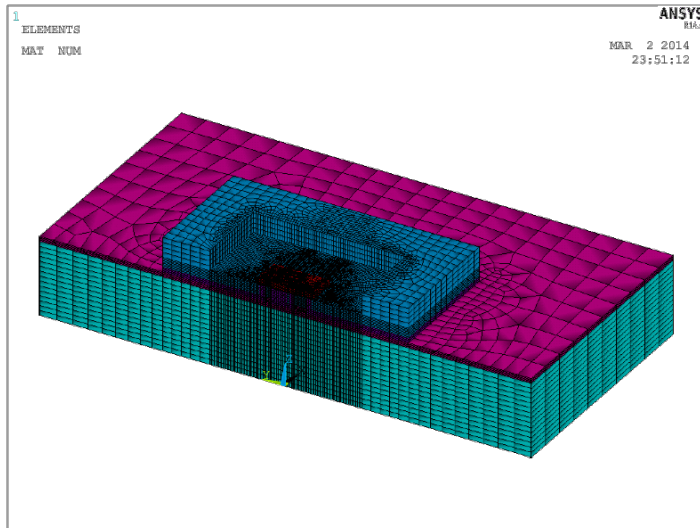
Equivalent Stress in Solder under ATC



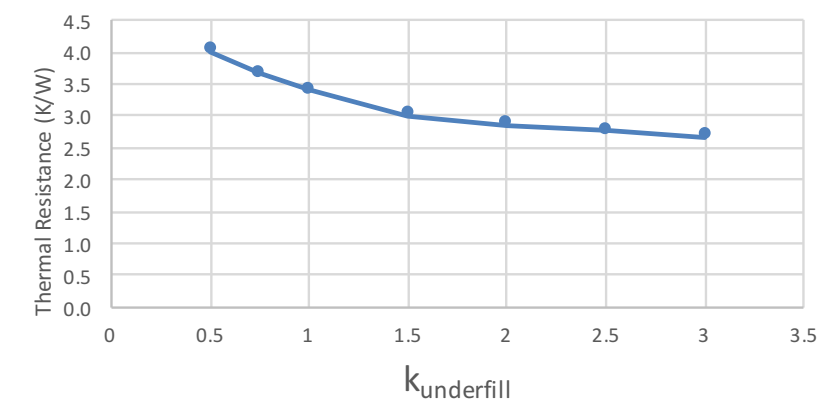
Inelastic Strain Versus Loading Cycle



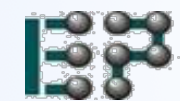
Thermal Simulation



Thermal Resistance vs. $k_{\text{underfill}}$

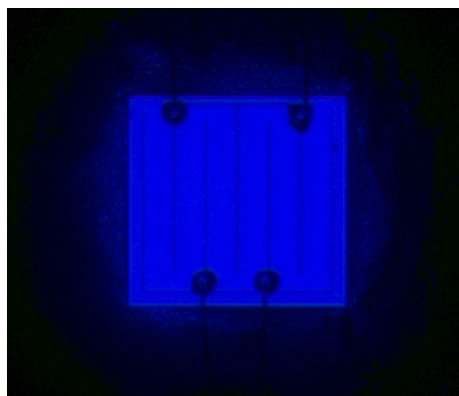


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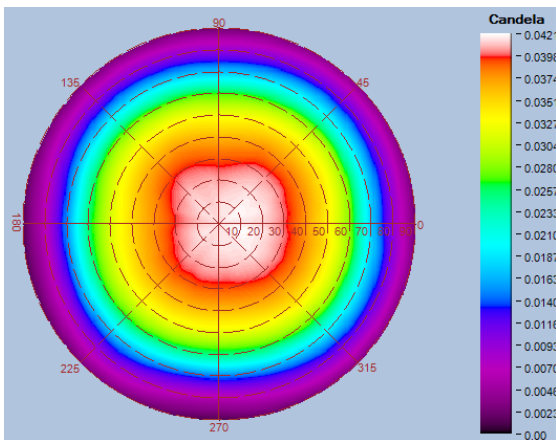


Optical Simulation

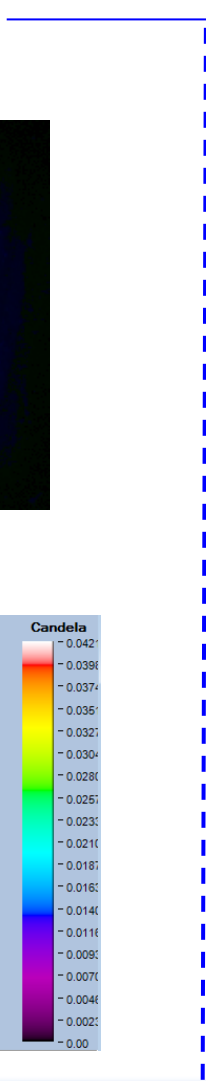
Source Imaging Goinophotometer



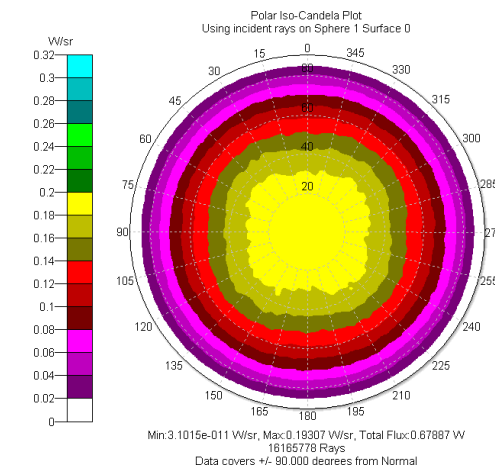
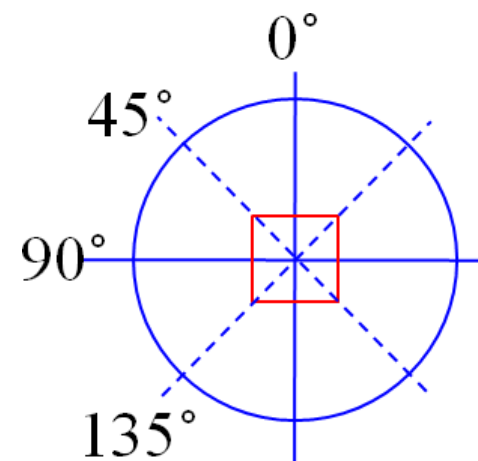
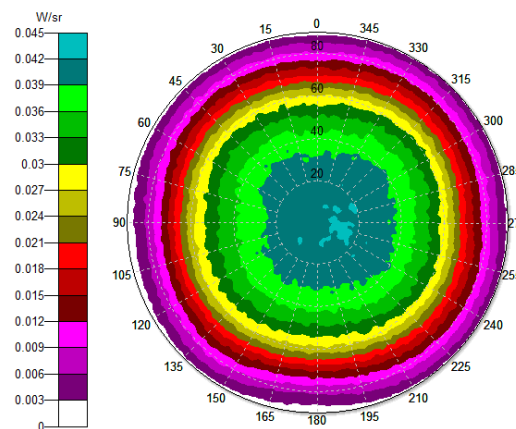
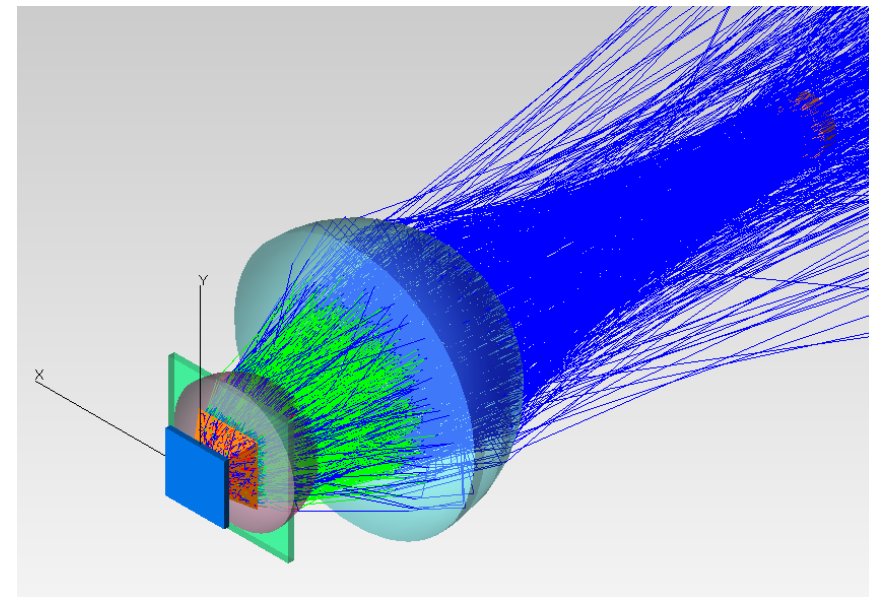
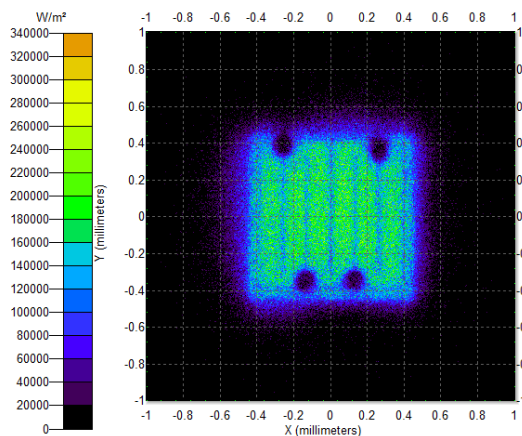
Bare chip



Source File



Ray Tracing Simulation



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